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INTERIM REPORT, CONTRACT NO. FA-WA-4178

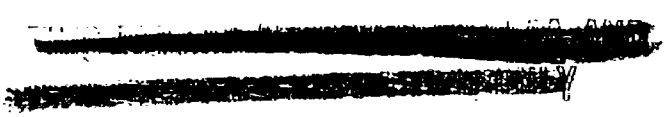
MODIFICATION OF ASR-4 RADAR INDICATOR

TO PROVIDE

BRIGHT DISPLAY OF RADAR, BEACON, ALPHA-NUMERIC AND SYMBOLIC DATA

SP21-A63

AUGUST 1, 1963



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FEDERAL AVIATION AGENCY
SYSTEMS RESEARCH AND DEVELOPMENT SERVICE

by

TEXAS INSTRUMENTS INCORPORATED
Apparatus Division
Dallas 22, Texas

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Project No. 425

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MODIFICATION OF ASR-4 RADAR INDICATOR TO PROVIDE BRIGHT DISPLAY OF RADAR, BEACON, ALPHA-NUMERIC AND SYMBOLIC DATA
by T. P. Kennedy, Project Engineer, 1 August 1963

Interim report composed of 58 pages, 26 illustrations, 4 tables

(Contract No. FA-WA-4178)

ABSTRACT

Design data for the bright display, readout trigger, and asynchronous beacon portions of the ASR-4 indicator modification were submitted and approved. Detail design and circuit evaluation of these items are largely complete. Preliminary specifications for the alpha-numeric display and message generator portions of the ASR-4 indicator modification have been received and are being reviewed. The basic scope of the program has not been changed except that the contract has been modified to provide for delivery of a two-console display subsystem rather than a one-console display subsystem.

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INTRODUCTION

This is the second quarterly report on Contract No. FA-WA-4178 to develop a modification kit for the ASR-4 subsystem. This kit will provide bright display of alpha-numeric and symbolic data, a readout trigger function, display of asynchronous beacon data, and a message generator keyboard.

Revised design data for the bright display, readout trigger and asynchronous beacon portions of the modification kit were submitted for review on 17 May 1963. Representatives of Texas Instruments and the FAA met to discuss revisions to this data during the week of June 5-12, 1963. This data, with revisions agreed to in the meeting, was approved on June 21 and Texas Instruments is proceeding with design and fabrication of equipment under this portion of the program.

The alpha-numeric display and message generator portions of the modification kit were under a partial stop order during May and June because of impending changes in the computer interface and message format specifications. The stop order expired on 30 June 1963 and preliminary design has proceeded during the month of July based on preliminary interface specifications for the UNIVAC 1218 Computer. Texas Instruments received a draft of Addendum No. 2 to Engineering Requirement ER-D-406-45 on 19 July 1963. This addendum redefines the message format requirements for alpha-numeric and symbolic display and the message generator keyboard.

I. DIRECT VIEW STORAGE TUBE MODIFICATION

A. Detail Design.

Two departures have been made from the design infromation described in the Interim Report of 1 May 1963; they are as follows:

(1) The 5-kilocycle dc-to-dc converter for the high voltage power supply has been abandoned in favor of a 60-cycle supply because investigation revealed that no transformer space could be saved, and space saved by the use of smaller filter capacitors at 5 kilocycles would not be as great as the space required by the 5-kilocycle generator.

(1) The prf on the mode 1 erase pulse generator has been doubled by changing the input from the cursor trigger (approximately 30 pps) to the radar deadtime trigger (approximately 1200 pps) fed through a divider circuit which will divide by 20. This change has been made to preclude the possibility of flicker which is noticeable on the DVST if a 30-pps erase pulse is used.

Figure 1 is a schematic diagram of the high voltage power supply. A thermal time delay of 30 seconds is provided so that the regulator tube heaters can reach operating temperature before high voltage is applied. Silicon rectifier stacks are used in a half-wavecircuit for the -4.9-kilovolt supply, and in a voltage doubler circuit for the +10-volt supply. Conventional shunt regulator tubes are used. It is planned to use the +10-kilovolt regulator tubes to act as the shunt tubes for lowering view screen potential during erase time.

Figure 2 is the schematic diagram of the DVST erase, control, and protective circuits. Sheet 1 shows the mode 2 erase pulse generator, an amplifier for the mode 1 erase pulse, and the range switch sensing flip-flop which triggers mode 2 erase when the range switch is moved from one position to another. Sheet 2 shows the mode 1 erase pulse generator and the backing electrode reverse current detector circuit. Sheet 3 shows the sweep rotation sensing circuit, the flood gun cathode current sensing circuit, the sweep sensing circuit, and the flip-flop which turns off video and unblanking.

Most of the schematics are easily followed by referring to SK425-4, page 4 of Interim Report dated 1 May 1963. This drawing includes a block diagram of the erase, control, and protective circuits. The flood gun cathode current is sensed by feeding the cathode to the summing junction of an operational amplifier and choosing the feedback resistor so that the output of the operational amplifier is equal to -2 volts per milliampere input. This output is shifted by means of a zener diode and fed to the flip-flop which turns off video and unblanking.

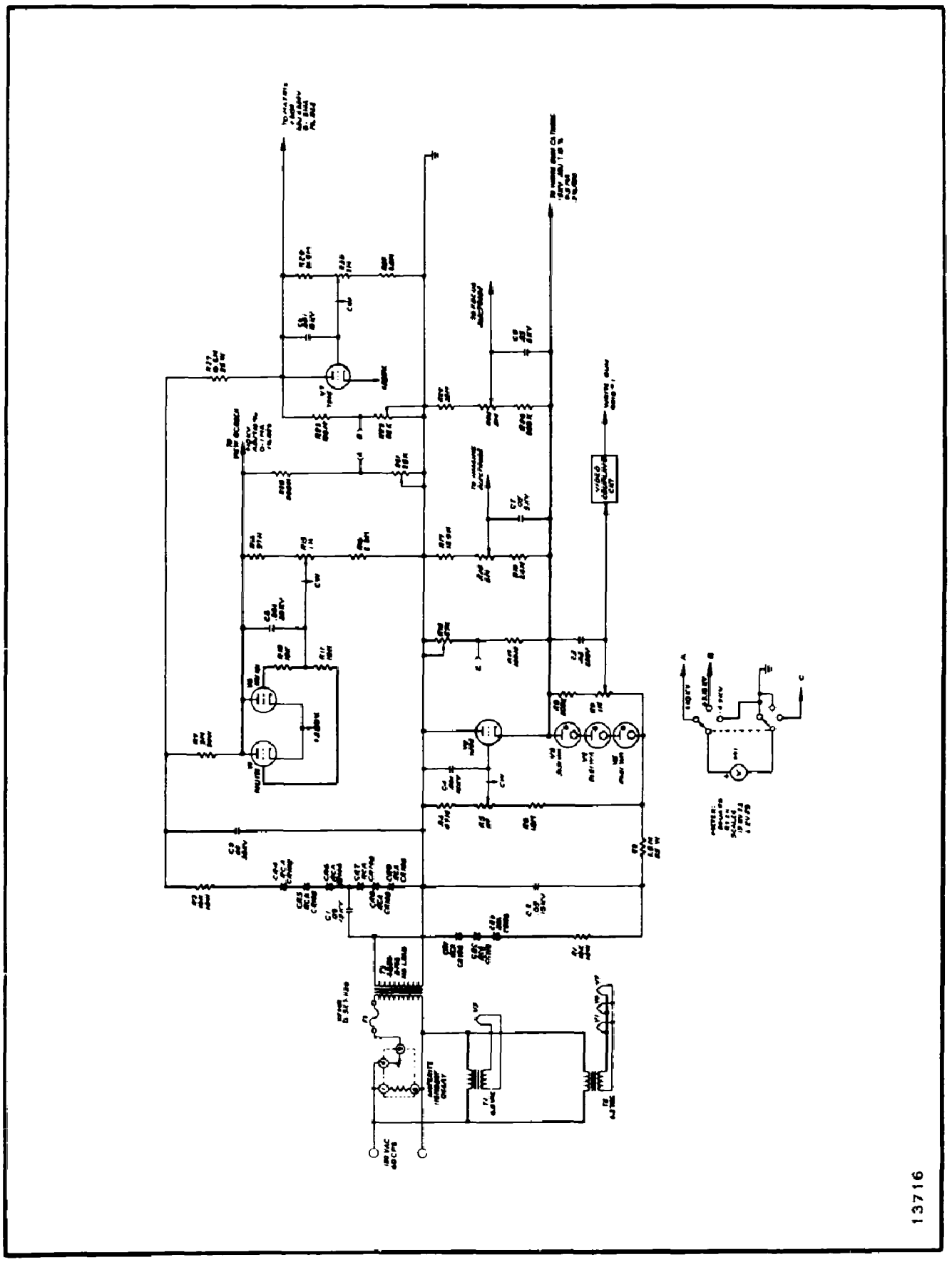

Figure 1. High Voltage Power Supply Schematic Diagram

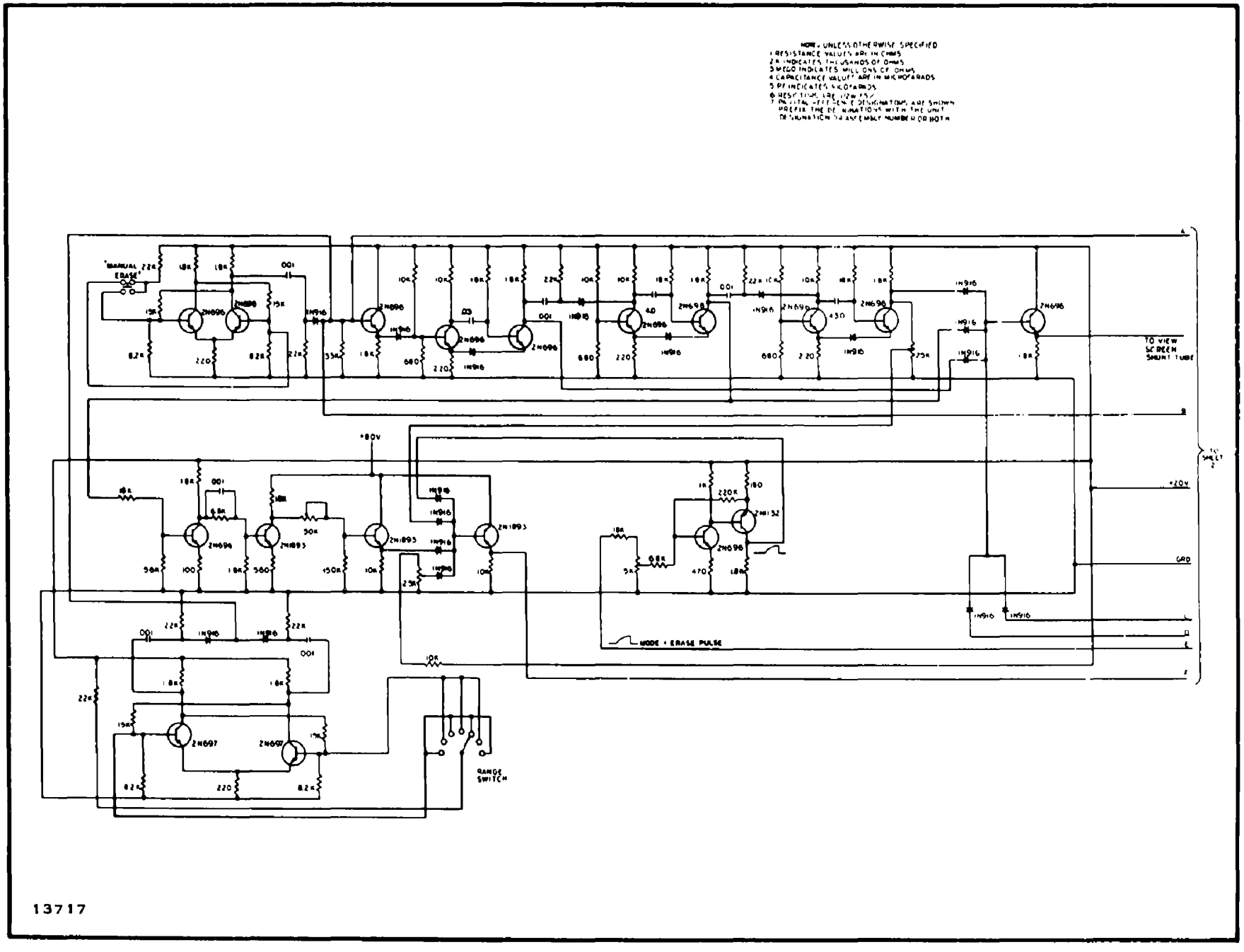

Figure 2. Erase and Protective Circuit Schematic Diagram (Sheet 1 of 3)

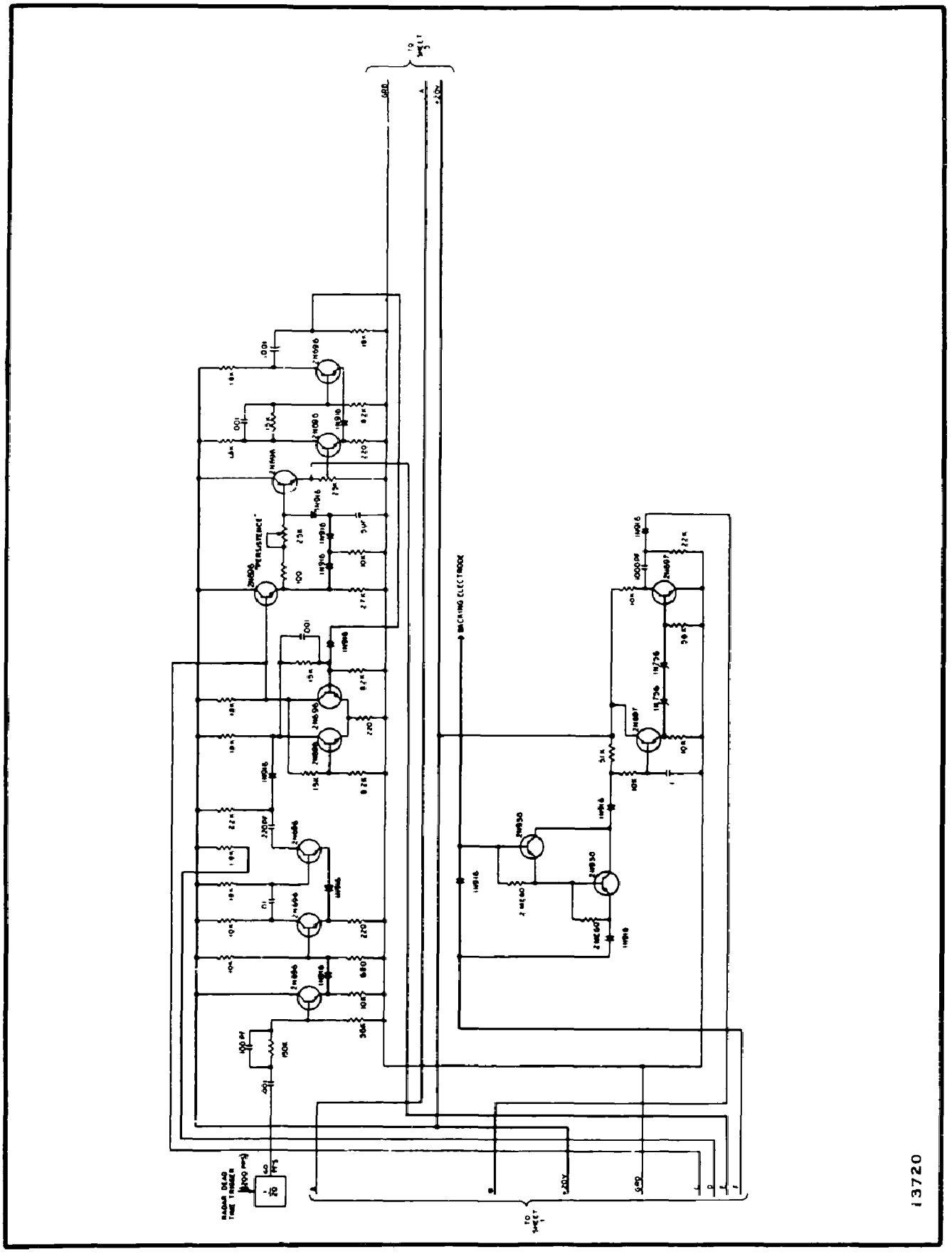

Figure 2. Erase and Protective Circuit Schematic Diagram (Sheet 2 of 3)

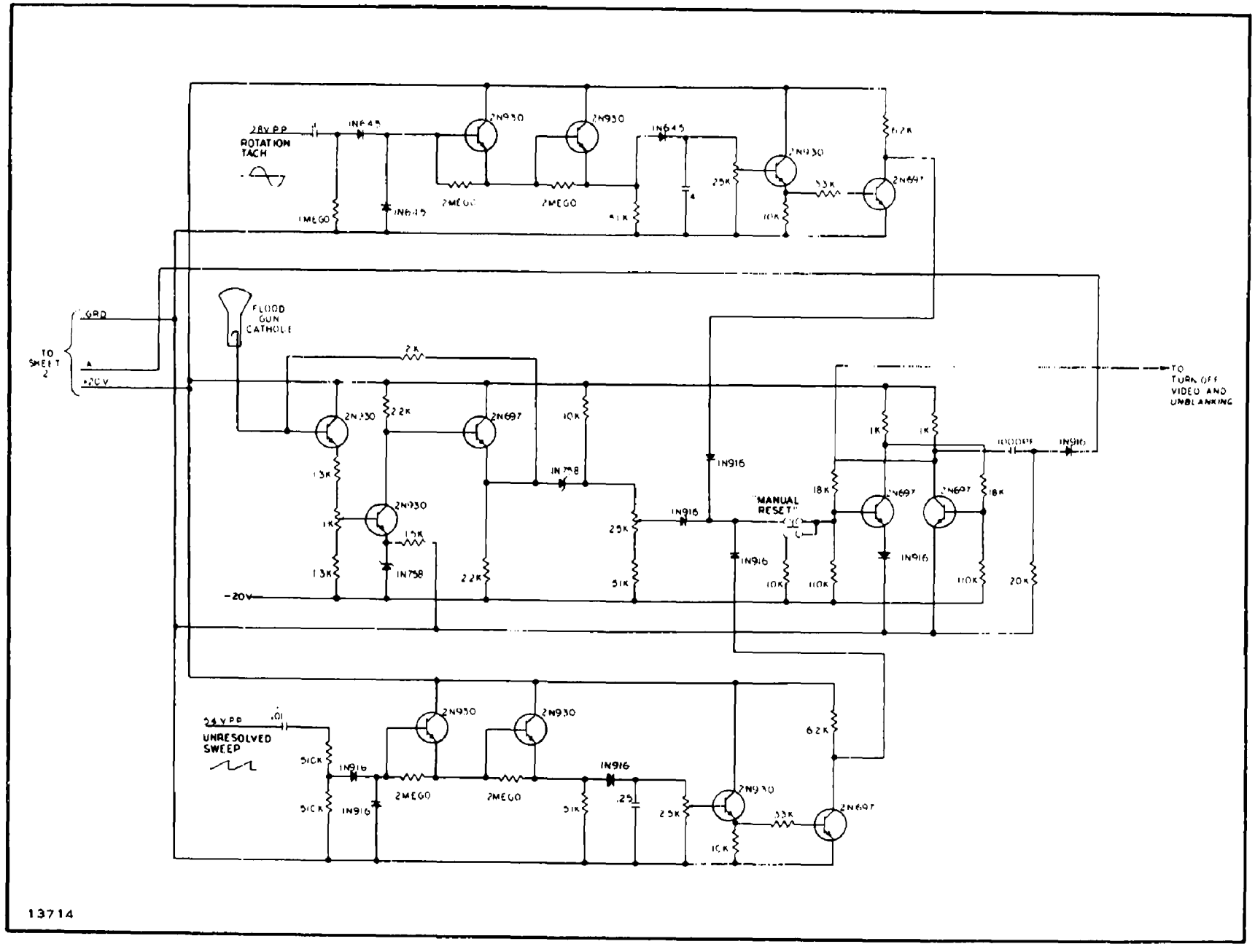

Figure 2. Erase and Protective Circuit Schematic Diagram (Sheet 3 of 3)

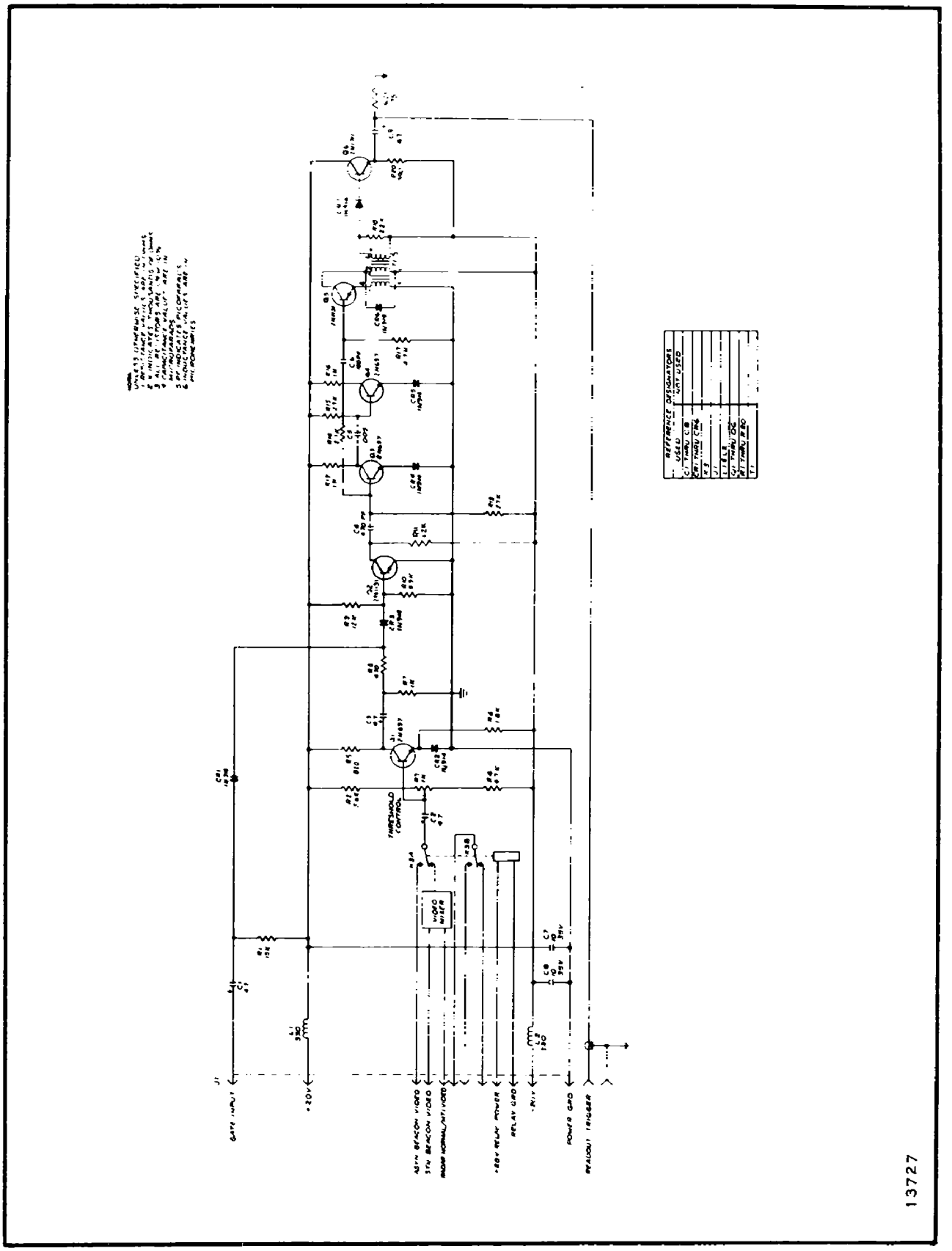

Figure 3. Readout Trigger Generator Schematic Diagram

B. Status of Direct View Storage Tube Modification.

All of the circuits shown in Figures 1 and 2 have been breadboarded and operate satisfactorily. Although the circuits cannot be fully developed until the DVST is received and put into operation, it is felt they will be able to operate the DVST safely. Breadboard construction remaining to be done before the DVST is received consists of:

(1) Interface between mode 2 erase generator and view screen shunt tubes.

(2) Video coupling circuit

(3) Flood gun collimating bias circuits.

No difficulty is anticipated in these circuits, and they should be completed well ahead of DVST delivery. Rewiring of the console for the DVST is underway.

II. READOUT TRIGGER MODIFICATION

A. Detail Design.

1. Slew Dot Generator (Figure 3).

Dead time trigger is applied simultaneously to slew dot delay generator Q1 and Q3, and to slew dot deflection gate generator Q2 and Q4, both of which are monostable multivibrators. The output waveforms from the slew deflection gate generator are applied to the bases of slew deflection gate drivers Q5 and Q6 through resistors R15 and R36, respectively. The collector waveforms from slew deflection gate drivers Q5 and Q6 are applied simultaneously to the N-S slew deflection gate consisting of diodes CR8 and CR13, and to the E-W slew deflection gate consisting of diodes CR14 through CR19. The N-S slew deflection gate (diodes CR8 through CR13) operates as follows: The N-S dc slew voltage input from the N-S slew dot operational amplifier is applied to the junction of diodes CR10 and CR11. In the quiescent condition, the anodes of diodes CR10 and CR12 are biased to approximately −15 volts since diode CR8 is forward biased through resistors R27 and R24; the cathodes of diodes CR11 and CR13 are biased to approximately +15 volts since diode CR9 is forward biased through resistors R25 and R28. As a result, diodes CR10, CR11, CR12 and CR13 are biased off, preventing the dc slew voltage input from being present at the N-S slew deflection voltage output (the junction of diodes CR12 and CR13).

Dead time trigger as applied to slew deflection gate generator (Q2 and Q4) generates a gate which is approximately 45 microseconds in duration and which is applied to slew deflection gate drivers Q5 and Q6. The resultant positive going output from the collector of Q5 is applied to the cathode

of diode CR8 through capacitor C10, biasing CR8 off for the duration of the gate. The negative-going output from the collector of Q6 is applied to the anode of diode CR9 through capacitor C11, biasing CR9 off for the duration of the gate. Diodes CR10, CR11, CR12, and CR13 are now forward biased into conduction through resistors R27 and R28. Because the forward voltage drops across diodes CR10 and CR12 are equal and the forward voltage drops across diodes CR11 and CR13 are also equal, the N-S dc slew voltage as applied to the junction of diodes CR10 and CR11 appears as an output voltage at the junction of diodes CR12 and CR13. The gated N-S slew deflection voltage output is fed to N-S Resolver Amplifier FA-4822 in Console Equipment Assembly FA-4821.

The E-W slew deflection gate (diodes CR14 through CR19) operates in the same manner as that outlined for the N-S slew deflection gate (diodes CR8 through CR13), the gated E-W slew deflection voltage output at the junction of diodes CR18 and CR19 being fed to the E-W Resolver Amplifier FA-4822 in Console Equipment Assembly FA-4821.

The dead time trigger applied to the base of Q1 causes slew dot delay generator Q1 and Q3 to generate a positive-going gate which is approximately 40 microseconds in duration. This waveform is differentiated by capacitor C7 and resistor R16, the negative-going trailing edge being fed to the base of Q7 through diode CR7. The resultant positive-going pulse at the collector of Q7 is fed to the crt unblanking circuits from emitter follower Q8.

2. Slew Voltage Generator (Figure 4).

The slew dot freeze circuits consist of a variable timer, Q4, Q5, Q6, and a pulse stretcher/relay driver, Q1, Q2, and Q3. In quiescent operation, relays K3, K4, and K5 are open while realys K1 and K2 remain normally closed. Timing capacitor C3 is held to negligible potential by one set of K3 contacts. Momentary closing of the slew dot joystick enter button closes relay K3 which locks in the closed position through one set of contacts. Timing capacitor C3 is now connected through the other set of K3 contacts to resistors R4 and R7 which comprise the resistor portion of the RC timing circuit. The charging potential on capacitor C3 is applied to the gate of a field effect transistor which is used as a source follower. The charging voltage across C3 appears as an output from field effect source follower Q4 which drives Schmitt trigger circuit Q5 and Q6. Capacitor C3 charges to a point at which Q5 conducts, turning off Q6 and deenergizing K2 which in turn deenergizes K3. Resistor R4 thus controls the time during which K3 is closed.

Gate outline pulses are applied to integrator circuit R8 and C1, through diode CR1. The voltage across C1 is fed to the gate of source follower field effect transistor Q1, the output of which is coupled to Schmitt trigger circuit Q2 and Q3. In quiescent operation relay K1 is closed because Q3 is conducting. The discharge time of C1 through R8 is such that each time a gate outline video pulse is applied to C1 through diode CR1, Q2 of the Schmitt trigger circuit is biased on for approximately 900 microseconds, turning Q3 off for this period and deenergizing relay K1.

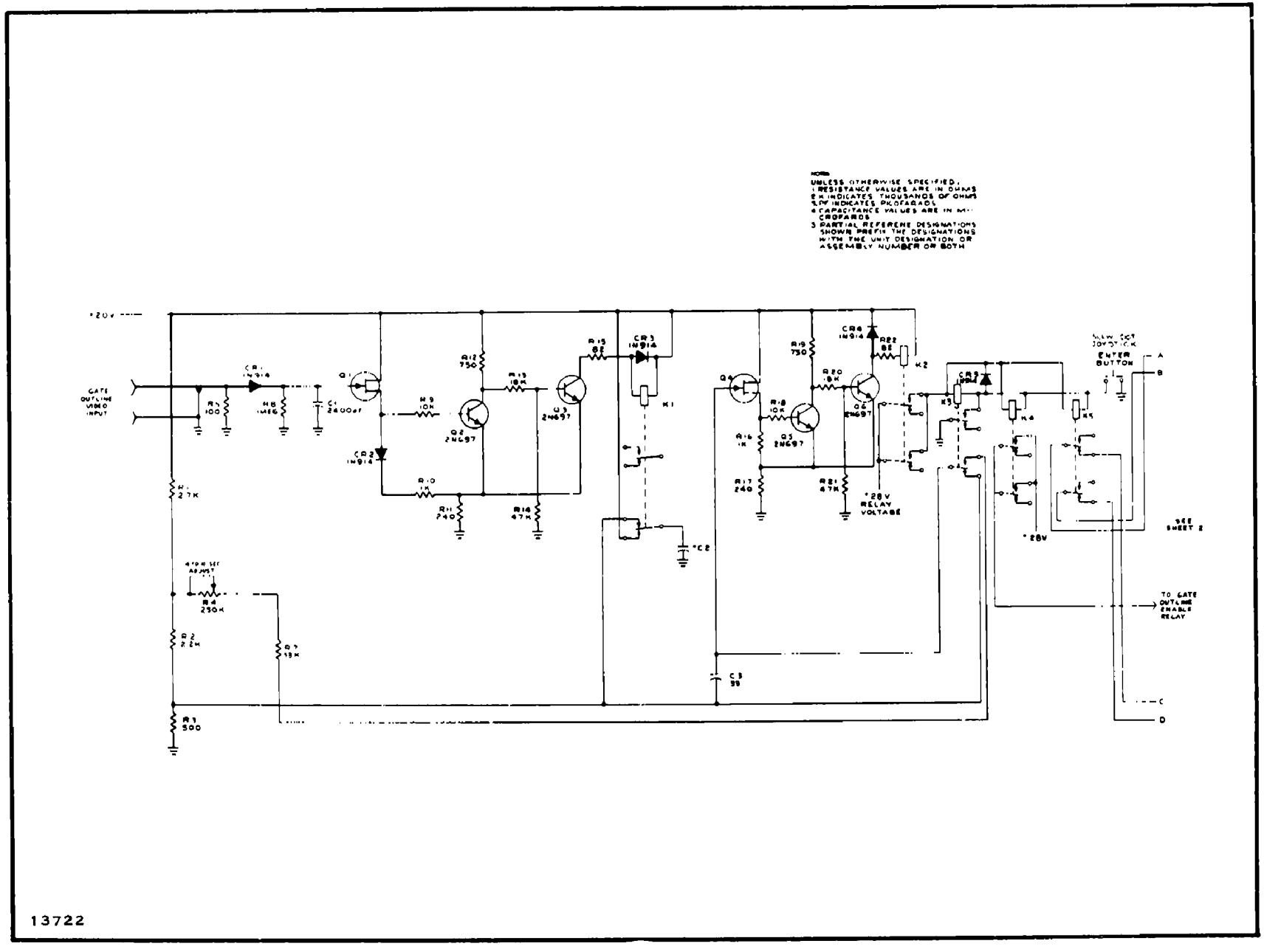

Figure 4. Slew Voltage Generator Schematic Diagram (Sheet 1 of 2)

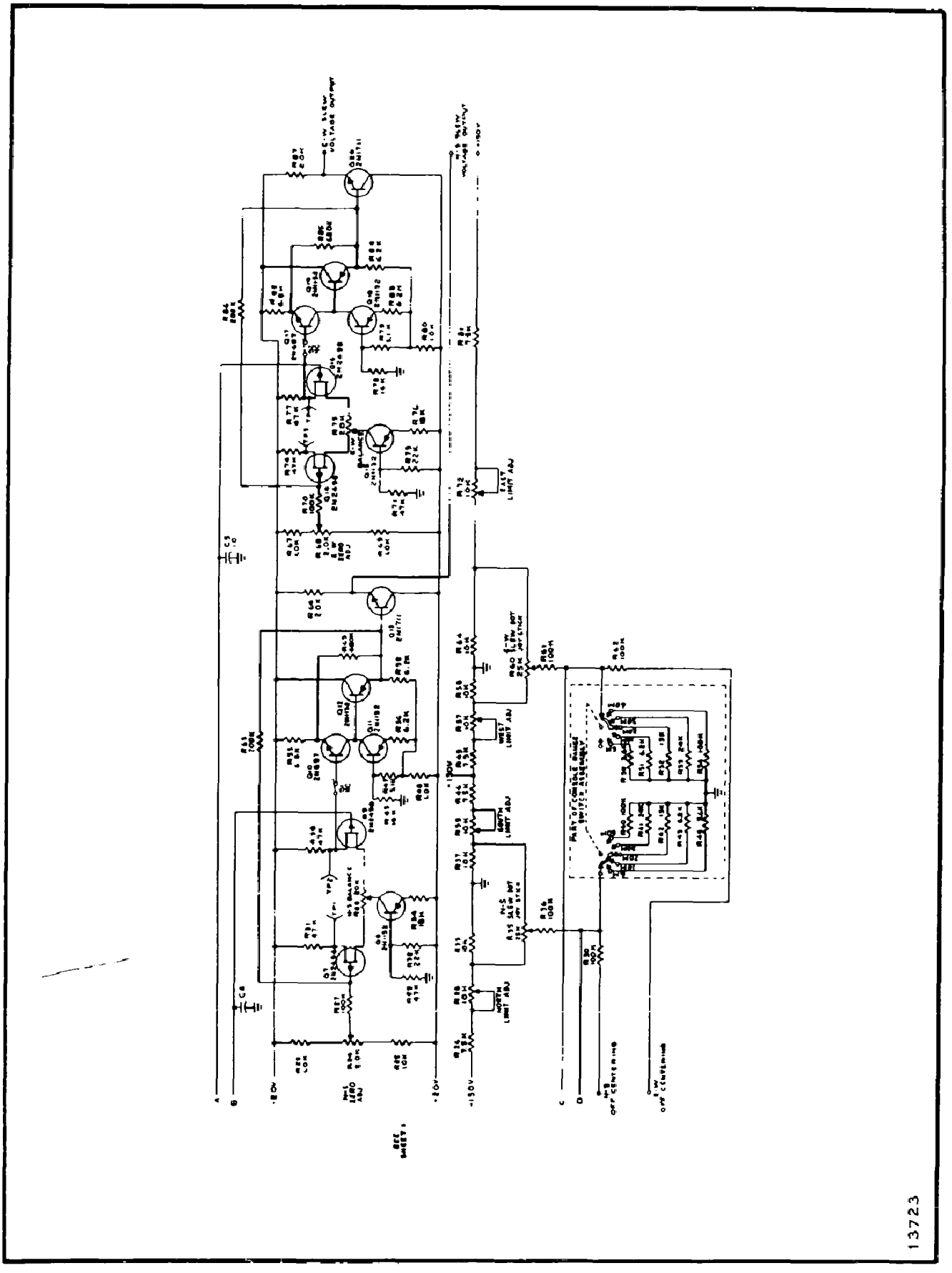

Figure 4. Slew Voltage Generator Schematic Diagram (Sheet 2 of 2)

When relay K1 is deenergized, capacitor C2 is charged to +20 volts through one set of contacts on K1 and is held in this condition as long as a gate outline video pulse appears at the input during each radar sweep. 900 microseconds after the last gate outline video pulse C1 discharges through R8 to the point where Q2 turns off, Q3 is again turned on, and relay K1 is reenergized. The positive voltage across C2 is then applied to the junction of R3 and C3 through relay K1 contacts, raising the gate voltage of field effect transistor Q4. Q4 then causes Q5 to conduct and Q6 to turn off, deenergizing relay K2 which in turn deenergizes relay K3. K3 discharges C3 which returns Q6 to its quiescent conducting state, reenergizing relay K2.

3. Slew Dot Freezing Circuits (Figure 5).

a. Origin of Sweep Enclosed By Gate Outline. - Depressing the enter button on the slew dot joystick closes relay K3 which holds in the energized position through one set of contacts. The other set of contacts applies the +10-volt charging potential to timing capacitor C3. The gate outline enable relay is energized simultaneously with relays K3 and K4, enabling gate outline video, which, appearing at the input to the pulse stretcher and relay driver (Q1, Q2, and Q3) deenergizes relay K1, charging capacitor C2. Since a gate outline video pulse occurs every sweep, relay K1 is held in the deenergized position. Relay K5, also energized simultaneously with relay K3, removes the slew dot joystick N-S and E-W voltages from the inputs to the respective slew voltage operational amplifiers allowing the input capacitors of these operational amplifiers to remain charged at the potentials analogous to the frozen joystick coordinates. After 4 to 10 seconds, as determined by timer control R4, relay K2 deenergizes, deenergizing relays K5, K4, and K3, once more applying the slew dot joystick N-S and E-W voltages to the respective operational amplifiers, disabling gate outline video, reenergizing relays K1 and K2, thus completing the slew dot freezing and timing cycle.

b. Gate Outline Centered Away From Sweep Origin. - Depressing the enter button on the slew dot joystick closes relay K3 starting the 4 to 10 second variable timing cycle, relay K4, enabling gate outline video, and relay K5 freezing the slew dot joystick electrical coordinates at the inputs to the slew voltage operational amplifiers. When gate outline video appears at the input of pulse stretcher/relay driver circuit Q1, Q2, and Q3, relay K1 is deenergized, charging capacitor C2 to +20 volts. One sweep after the final gate outline video pulse appears at the input to the pulse stretcher, relay K1 again energizes, resetting 4 to 10 second variable timer Q4, Q5, and Q6, deenergizing relay K3 which reenergizes relay K2, completing the slew dot freezing and timing cycle.

The N-S slew voltage operational amplifier referenced in the above discussion consists of transistors Q7 through Q13 and the E-W slew voltage operational amplifier consists of transistors Q14 through Q20.

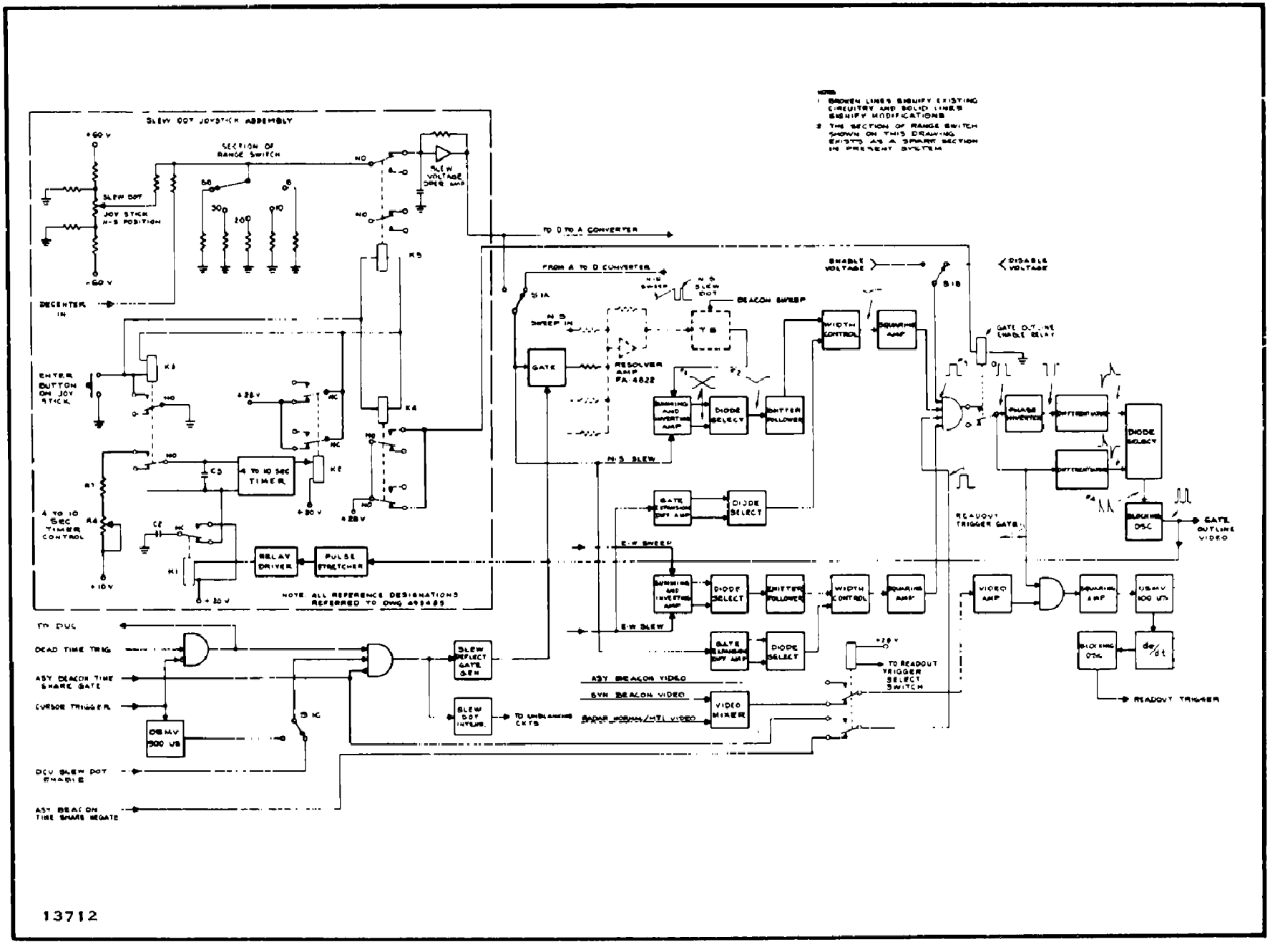

Figure 5. Readout Trigger Functional Block Diagram

4. Gate Outline Generator.

Most of this circuit is the same as described in the Interim Report of 1 May 1963. The new schematic is shown in Figure 6, and the changes are as follows: (1) The width control differential amplifier which consists of Q1, Q2, and Q3 is included. R6 is the control for varying the expansion rate from one to five miles. The width control circuit has been modified slightly in order to simplify the squaring amplifiers which follow. The width of the triangular signal is controlled by comparing it with the output of the width control differential amplifier and by diode selecting the more negative voltage. (2) Separate blocking oscillators are used to generate the two video pulses in order to reduce the minimum width possible between the two pulses. If two blocking oscillators are not used, then the recovery time of the first pulse would blank out the second pulse when the gate width is narrow and the gate as printed on the crt would have part of the corners missing.

5. Trigger Generator Circuitry.

The new approach to this circuit as stated in the Interim Report of 1 May 1963 has been breadboarded and tested. The circuit met all specifications, with the exception of amplitude which was 1.5 volts low. This part of the specification can be easily met by increasing the supply voltage on the output emitter follower. The circuit was also tested using live video signals and satisfactory results were obtained with the threshold control set from grass level to 1.8 volts. A schematic diagram is shown in Figure 3.

The input video pulse has a maximum amplitude of two volts. The threshold control applies a negative bias to the first stage so that it will not conduct until the input signal overcomes this bias. Diode CR2 extends the range of the threshold control. The output of Q1 is gated with the beacon trigger gate and amplified by Q2. This output is differentiated and used to trigger a monostable multivibrator the pulsewidth of which is 100 microseconds. The leading edge of this pulse is used to fire a blocking oscillator and the output is fed to an emitter follower which feeds 300 feet of RG 59/U cable. A 75-ohm resistor is used in the emitter circuit of Q6 so that the cable impedance is matched for reflected signals.

B. Status of Readout Trigger Modification.

Detail design of the readout trigger modification is 90 percent complete. Besides a conventional video mixer, the remaining work primarily concerns the relay switches and logic circuits associated with some of the other modification groups. These circuits will be built as the modification groups are tied together as one system.

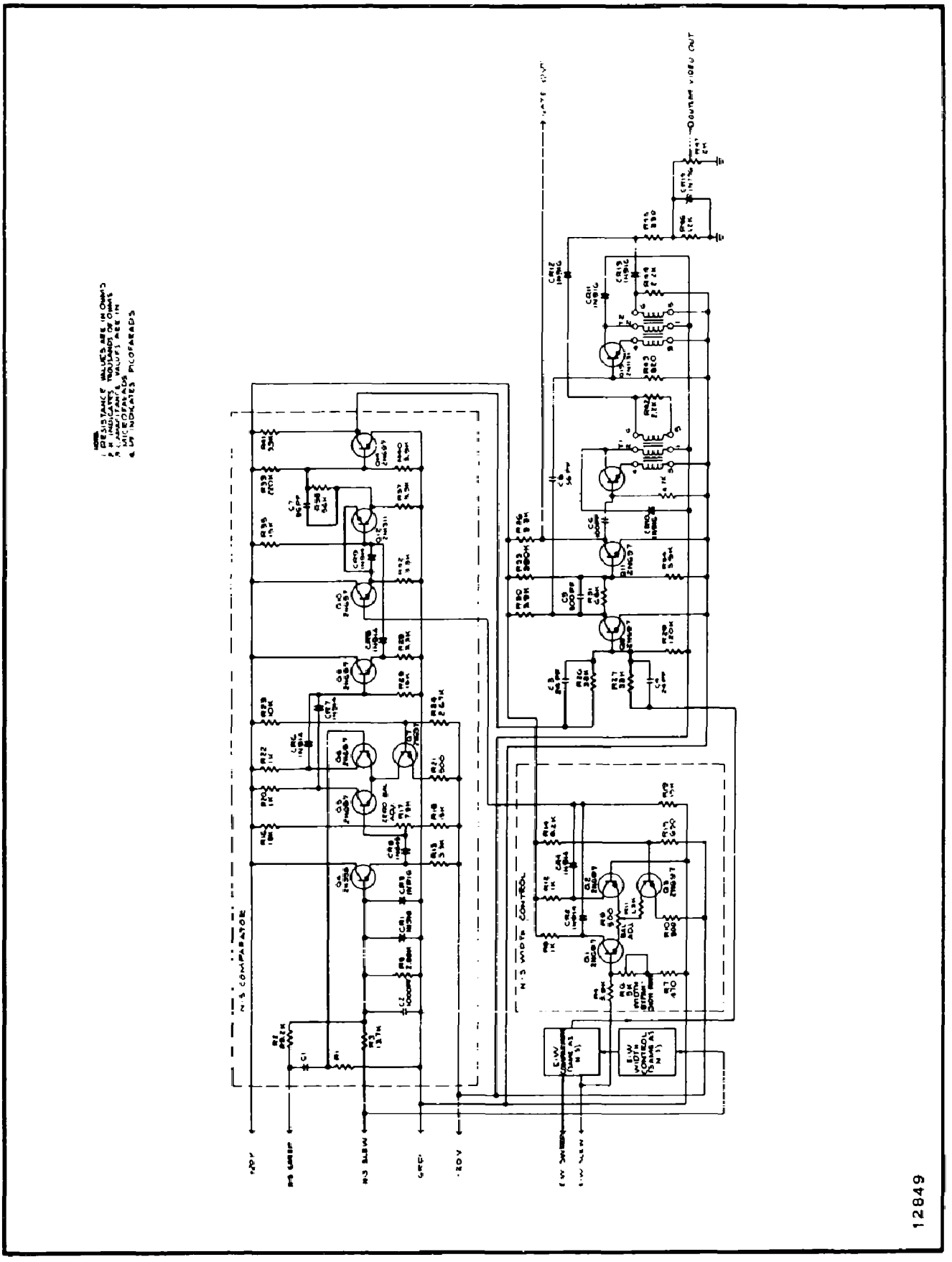

Figure 6. Gate Outline Generator Schematic Diagram

Improvements have been made on the gate outline generator, slew dot generator, and beacon trigger portions of the circuitry. An operational amplifier using field effect transistors in the differential amplifier stage has been breadboarded and tested. This amplifier has an input impedance which is high enough to hold the charge on a 1-microfarad capacitor to 99.8 percent for a period of 4 seconds. Also, the slew dot freezing circuitry and range switching has been breadboarded and tested.

III. ASYNCHRONOUS BEACON MODIFICATION

A. Objective.

There is no change in the objective for the design of the asynchronous beacon modification.

B. Design Approach.

Since the May 1 report certain changes in design approach have occurred. A new functional block diagram is shown in Figure 7, which includes the most recent changes. Voltage waveforms are included for clarity.

For the most part all functions are time shared as before. The method in some cases has changed. The video time share switch was originally a diode gate and has since been relocated and replaced by a bidirectional transistor gate. Previously, the time sharing of the sweep was to occur at the output of Resolver Amplifier FA-4822. A new approach has been taken wherein the switching is done ahead of the operational amplifier in FA-4822.

One major addition is the automatic fail-safe circuit. The original approach called for each gate to be fail-safe or be able to return to radar mode if the asynchronous beacon equipment failed during the asynchronous beacon time share period. This concept is replaced by a single fail-safe circuit on the basic asynchronous beacon time share gate generator. It is felt that this accomplishes the same purpose as the other approach, is just as reliable, and more economical.

C. Detail Design (Figure 8).

1. Asynchronous Beacon Time Share Gate Generator.

The asynchronous beacon time share gate generator is required to provide a gate that will enable the switching action between normal ASR-4 radar information and asynchronous beacon information.

Both a unipolar type and a bipolar type of bistable multivibrator were considered but the necessity for a negative voltage to insure cutoff of the logic circuits resulted in the choice of a bipolar multivibrator, Q18 and Q19, operating between +60 volts and -20 volts.

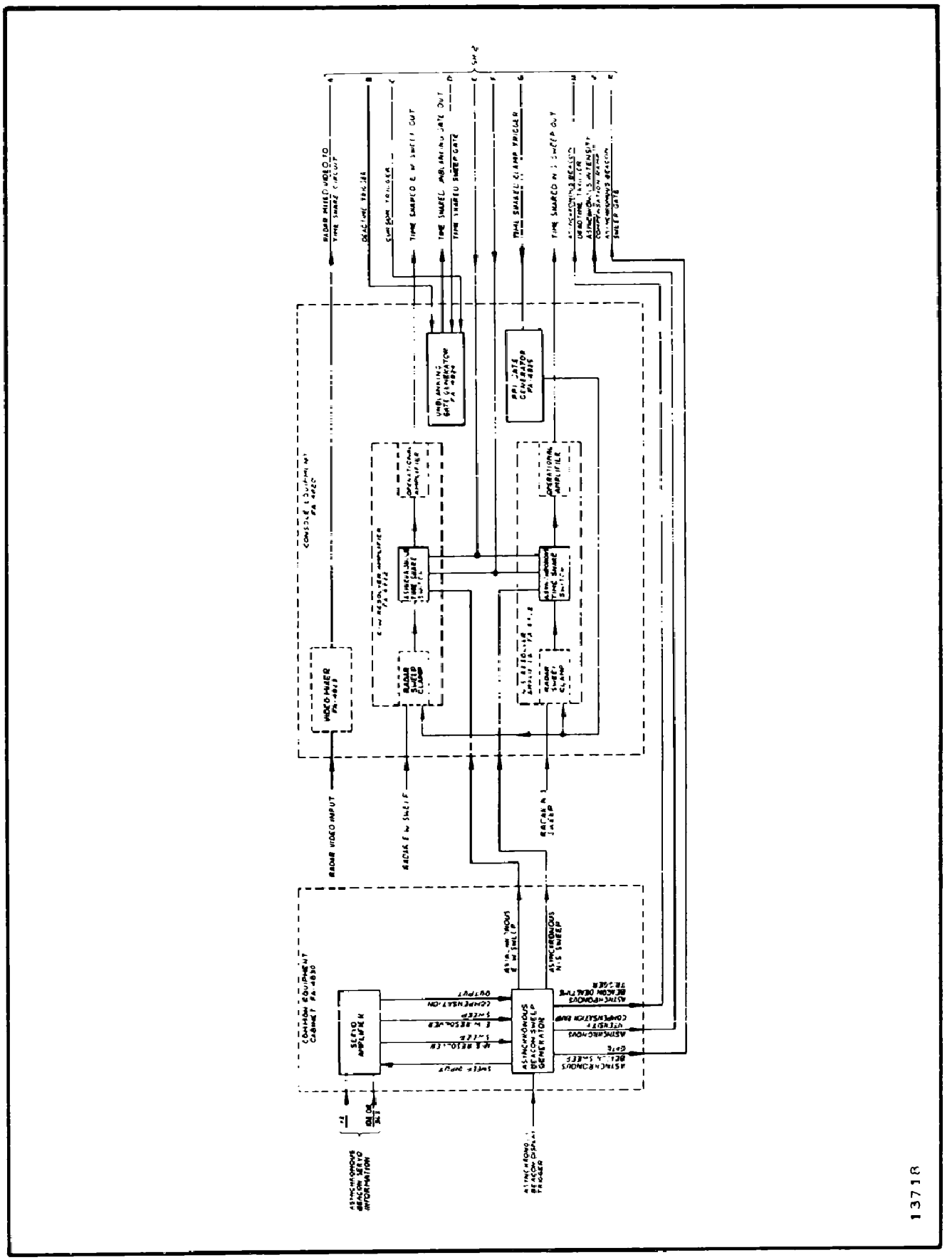

Figure 7. Asynchronous Beacon Functional Block Diagram (Sheet 1 of 2)

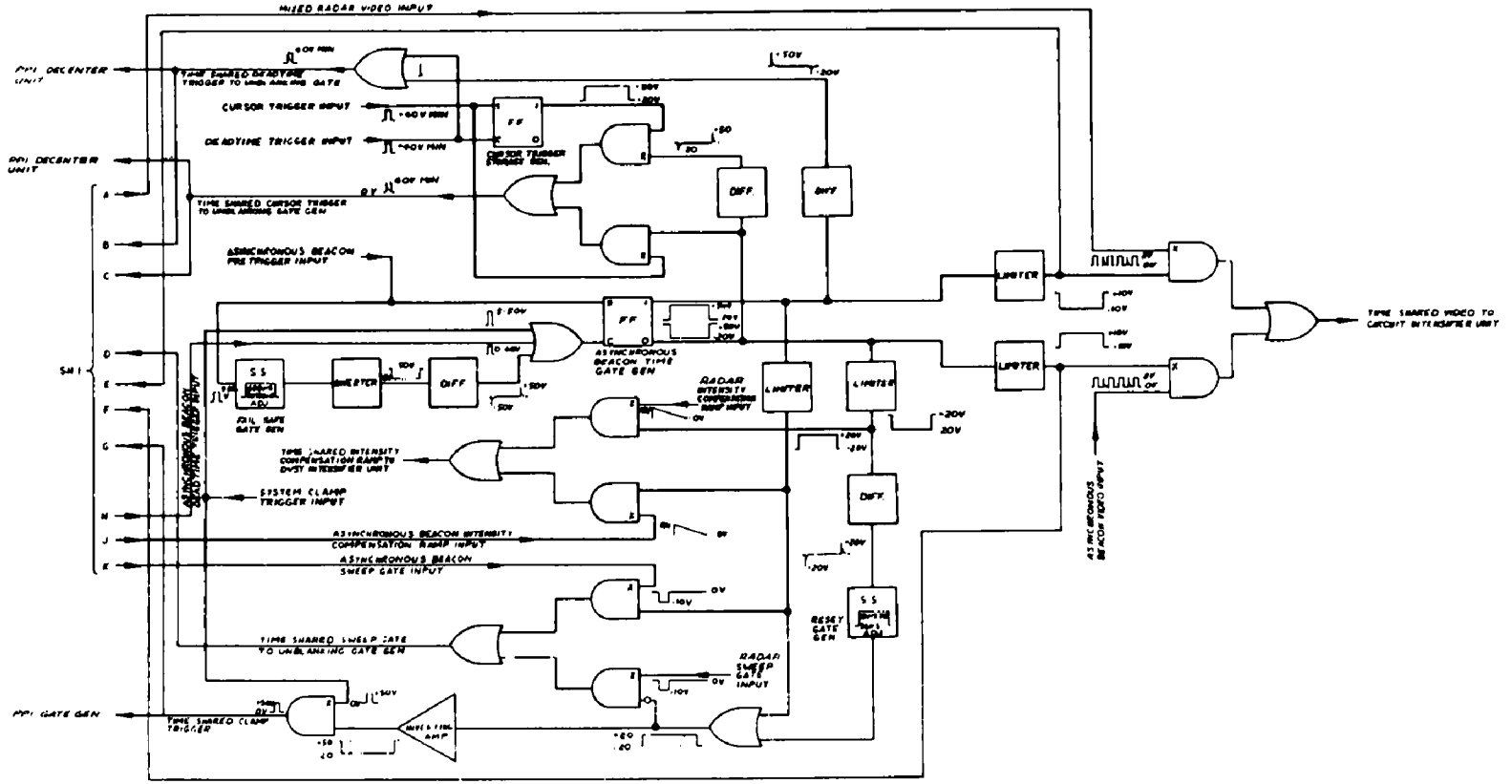

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Figure 7. Asynchronous Beacon Functional Block Diagram (Sheet 2 of 2)

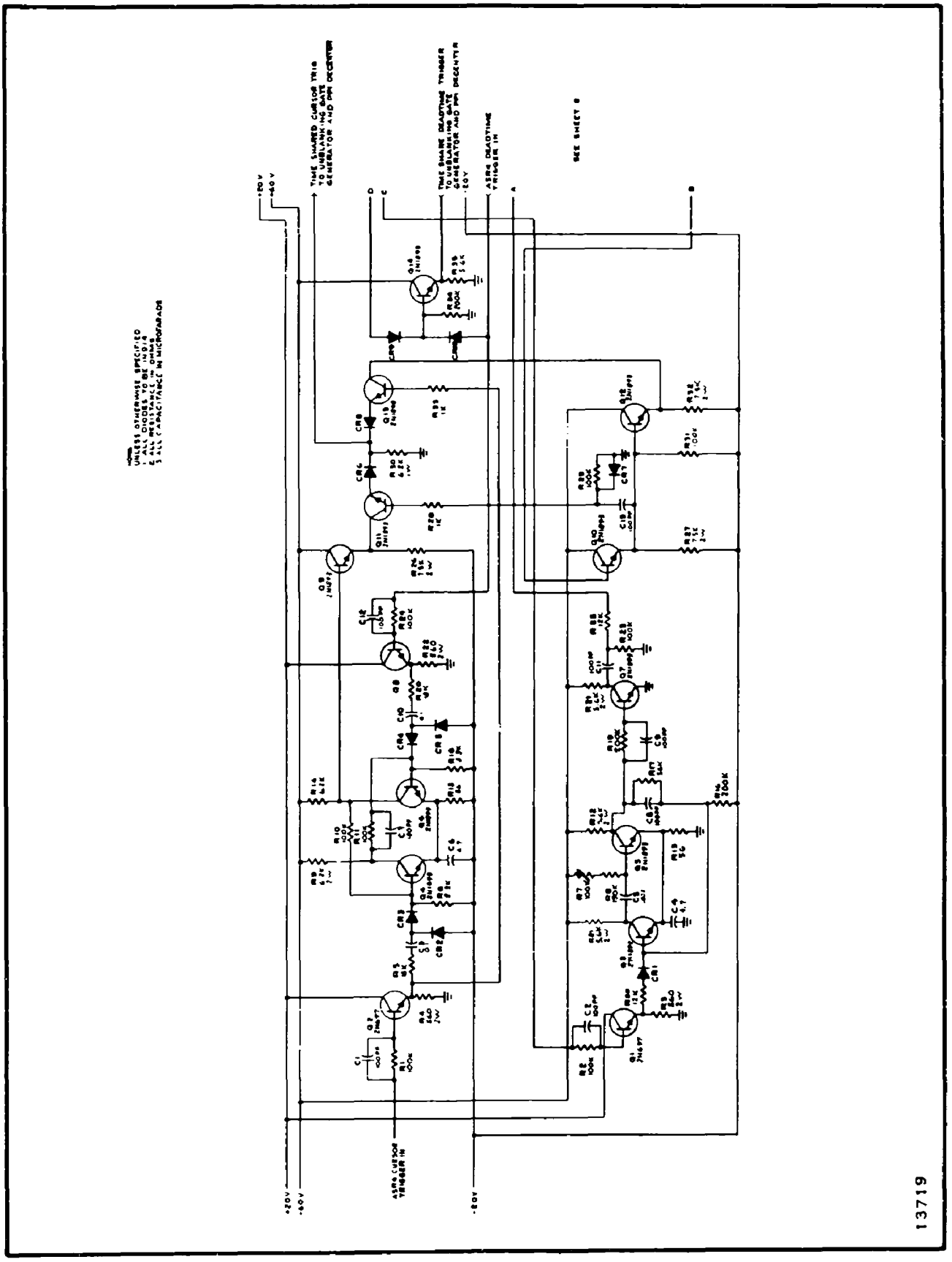

Figure 8. Asynchronous Beacon and Radar Time Share Logic Schematic Diagram (Sheet 1 of 2)

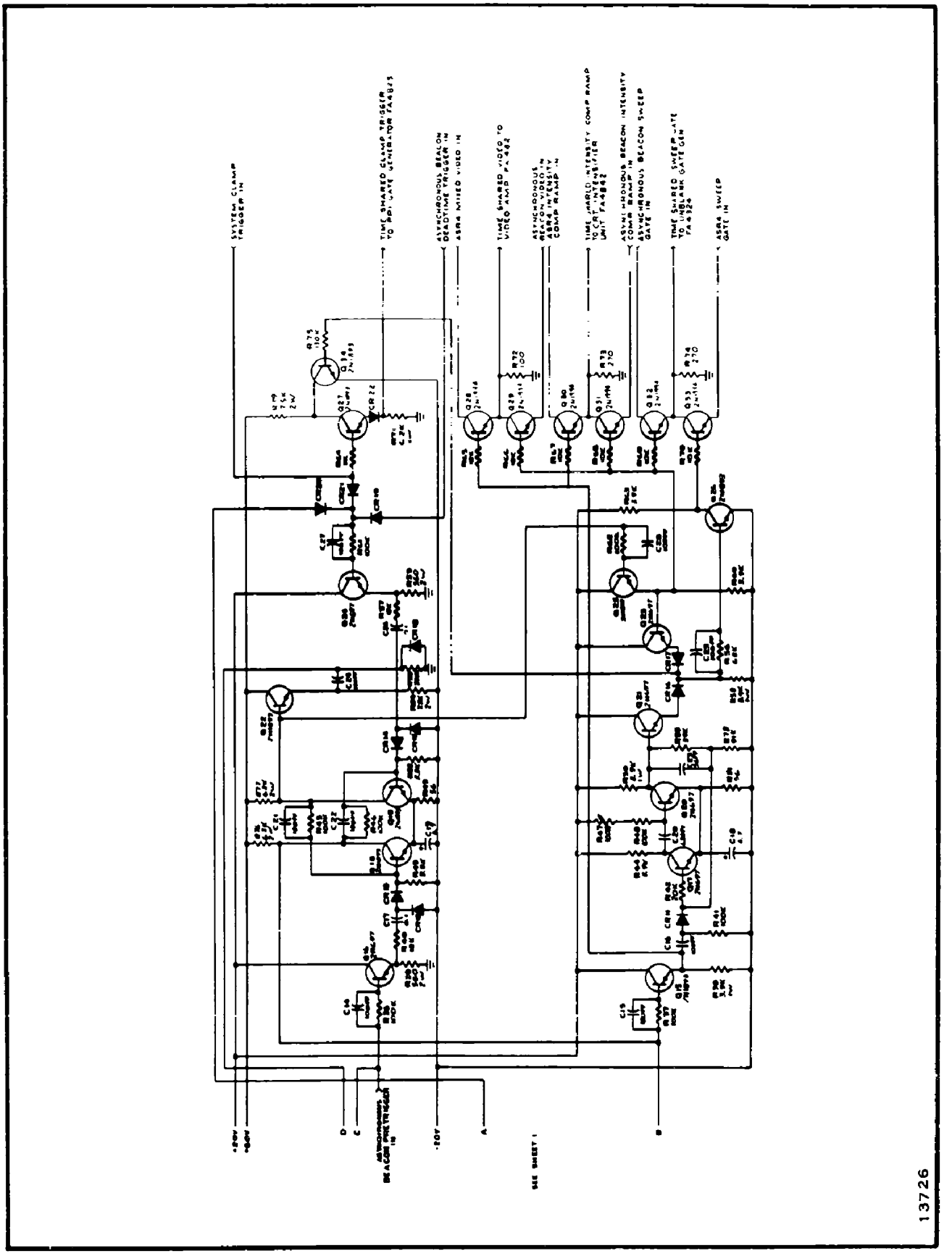

Figure 8. Asynchronous Beacon and Radar Time Share Logic Schematic Diagram (Sheet 2 of 2)

Input emitter follower limiters Q16 and Q24 are used for proper switching with triggers ranging in amplitude from 5 volts to 50 volts. If an input trigger has an amplitude of between 5 volts and 20 volts, the output of the emitter follower limiter is approximately equal to the input. If, however, an input trigger is greater than 20 volts, the output of the emitter follower limiter is limited to 20 volts.

An asynchronous beacon pretrigger is coupled through emitter follower limiter Q16, dc restored to -20 volts by C17 and CR12, and applied to the base of Q18. Q18 is saturated and Q19 is cut off.

The asynchronous beacon deadtime trigger, the system clamp trigger, and the automatic asynchronous beacon cut-off trigger are "ored" by CR19, CR21, CR20, and emitter follower limiter Q24. The resulting output trigger is dc restored to -20 volts by CR15 and C26 and applied to the base of Q19. This saturates Q19 and cuts off Q18.

The positive asynchronous beacon time share gate is taken from the collector of Q19 and the negative asynchronous beacon time share gate is taken from the collector of Q18.

2. Automatic Asynchronous Beacon Cut-off Circuit.

The possibility of an asynchronous beacon system failure during asynchronous beacon time requires a circuit that will automatically produce a trigger that will reset the asynchronous beacon time share gate to the normal ASR-4 radar position. An RC network with a slow rise time was considered and found to be unsuitable because of unstable timing. As a result, a monostable multivibrator, Q3 and Q5, was selected for better timing reliability.

The asynchronous beacon pretrigger is fed to an emitter follower limiter, Q1, of the same type as described in the time share gate gnerator section. The 5-volt to 20-volt trigger output causes the collector of Q5 to switch to approximately +60 volts.

The timing circuit consistings of R7, R8, and C5 causes the multivibrator to return to its stable state in 850 microseconds. The timing is made adjustable by potentiometer R7.

The positive gate from the collector of Q5 is inverted by Q7 and differentiated by R23 and C11 which results in a positive trailing edge trigger occurring 850 microseconds after the asynchronous beacon pretrigger. Thus, if no asynchronous beacon deadtime trigger or system clamp trigger occurs within 850 microseconds after an asynchronous beacon pretrigger, the asynchronous beacon time share gate generator will automatically be returned to the normal ASR-4 radar position.

3. Bidirectional Time Share and Reset Gates.

The requirement that the DVST remain blanked for 25 microseconds after the system switches from asynchronous beacon to normal ASR-4 radar information necessitates the generation of a 25 microsecond reset gate. Because the bidirectional time share logic circuits operate best with applied gates of -20 volts and +20 volts, the reset gate is generated by a monostable multivibrator, Q17 and Q20, operating between +20 volts and -20 volts.

The negative asynchronous beacon time share gate is fed to the input of emitter follower limiter Q15. The output of Q15 is limited at +20 volts and this bipolar gate is fed to the ASR-4 radar AND circuits in the bidirectional logic circuitry and to a differentiator, R41 and C16, which generates a positive trigger occurring at the end of asynchronous beacon time. This trigger switches the reset gate generator to its quasi-stable state and timing circuit R47, R48, and C20 returns the multivibrator to its monostable state in 25 microseconds. R47 is adjustable to insure proper timing of the output gate. The reset gate is fed to OR circuit Q21 and Q23 and is ORed with the positive asynchronous beacon time share gate. Q25 is an emitter follower limiter which limits the output gate to +20 volts. The output of Q25 is fed to the asynchronous beacon AND circuits in the bidirectional time share logic circuitry and to OR circuit Q21 and Q23.

The output of the OR circuit is inverted by Q26 and fed to the ASR-4 sweep gate AND circuit in the bidirectional time share logic circuits.

4. Bidirectional Time Share Logic Circuit.

Figure 9 is the basic schematic diagram of the 2N1994 AND transmission gate. The 2N1994 is an NPN Germanium Alloy junction transistor which has symmetrical collector-base and emitter-base junctions with respect to breakdown voltage and dc current gain. Therefore, if properly biased, it is able to pass signals of either polarity. The 2N1994 requires a positive gate greater than or equal to the signal level to pass the signal and a negative gate to inhibit the signal. Because of the symmetry of the transistor, the base current divides between collector and emitter in proportion to the collector and emitter impedances; and if a low signal source impedance is maintained, the output across R2 is essentially free of any gate caused pedestal. R1 is chosen so that the gate signal saturates the transistor during ON time. This makes the ON impedance of the transistor gate low, i.e., 3 to 8 ohms, and the gain of the stage is very close to one.

When the base applied gate signal is negative, both junctions are back biased and any signal applied at the collector is attenuated by the large back bias resistance. There is a small amount of high frequency feedthrough due to junction capacitance; however, the total OFF attenuation is still greater than 40 decibels.

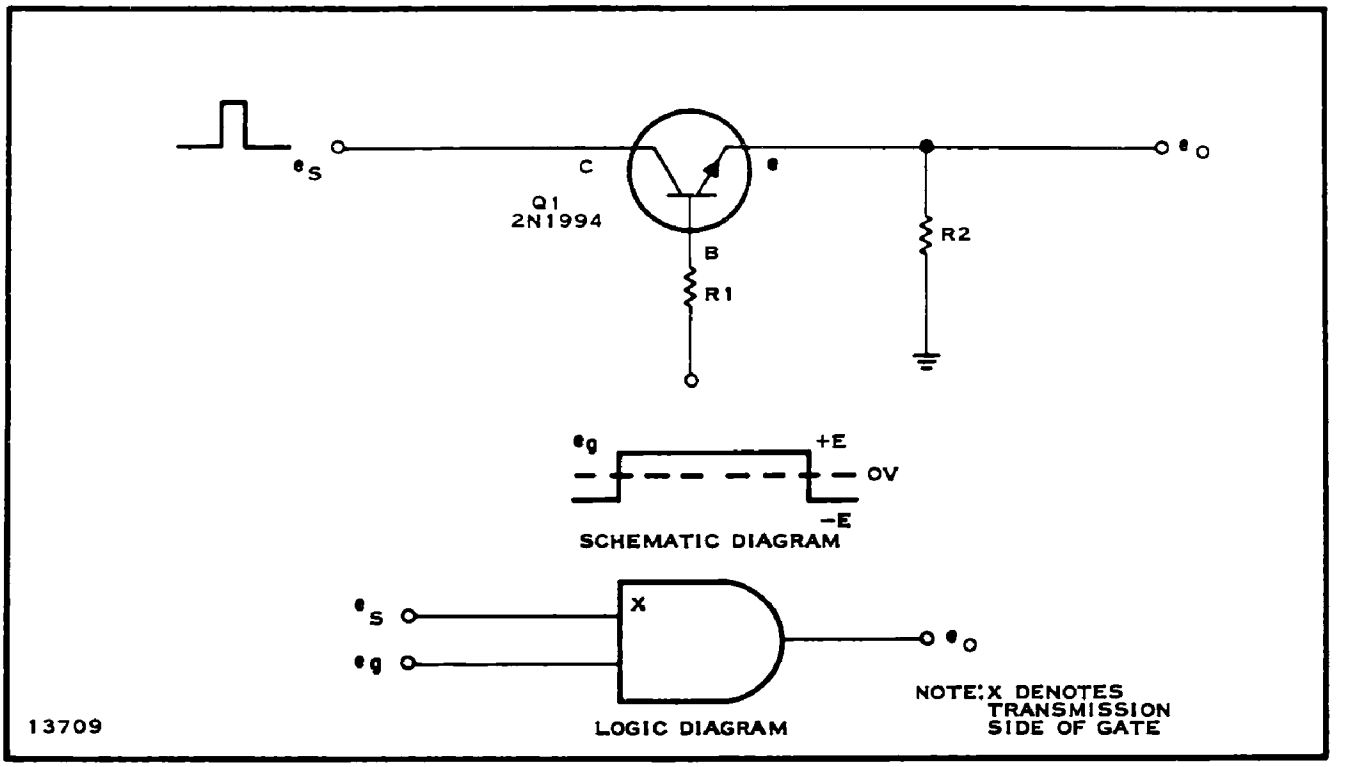

Figure 9. Bidirectional Transistor AND Gate

A time share logic switch is completed by using two 2N1994 AND circuits sharing a common emitter resistor as shown in Figure 10. The crosstalk between AND circuits is only the small amount due to the capacitive feedthrough of the OFF transistor. This configuration is used to time share the asynchronous beacon and ASR-4 radar information.

Q28 and Q29, shown in Figure 8, act as time sharing logic for ASR-4 and asynchronous beacon videos, while Q30 and Q31 time share the ASR-4 and asynchronous beacon intensity compensation ramps. Q32 and Q33 act to time share the ASR-4 and asynchronous beacon sweep gates. The base signal applied to Q33 is the negative asynchronous beacon and reset gate. Thus, the ASR-4 sweep gate is inhibited during asynchronous beacon time and remains inhibited for 25 microseconds after asynchronous beacon time.

5. Asynchronous Beacon Sweep Time Share.

Figure 11 shows the radar and asynchronous beacon sweep time share switches. The switches are essentially standard 6-diode gates; however, they are inserted at the summing point of the operational amplifier and thus operate as a current switch. The normal 6-diode gate requires a gate voltage as large or larger than the signal voltage but operating the gate, as shown in Figure 11, allows the gate voltage to be small in comparison to the signal voltage. A ±10 volt gate signal was chosen because it was easy to generate and meets the gate level requirements.

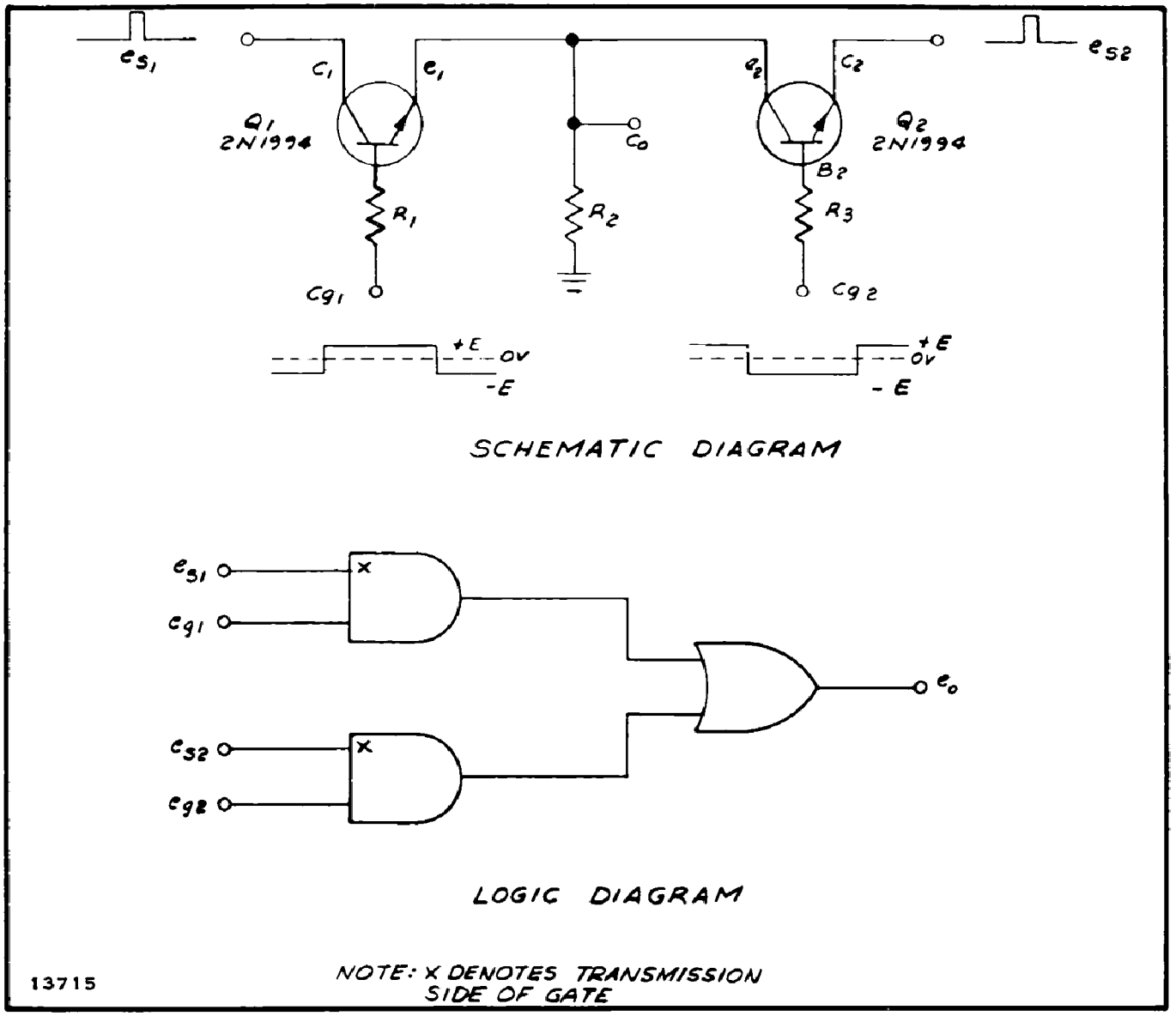

Figure 10. Bidirectional Time Share Switch

The time share circuits operate as follows. A positive gate voltage at CR1 and CR7 of S1 and a negative gate voltage at CR6 and CR12 of S2 will turn on the 6-diode gate. As shown in Figure 11, S1 receives control gates of opposite polarity to those of S2. Thus, when S1 is on, S2 is off and vice versa.

The radar sweep information is applied at summing resistors R1, R2, and R3 and the asynchronous beacon sweep information is applied at summing resistors R7 and R8 of S2. The output of the differential amplifier is the time shared sweep which is sent to the console.

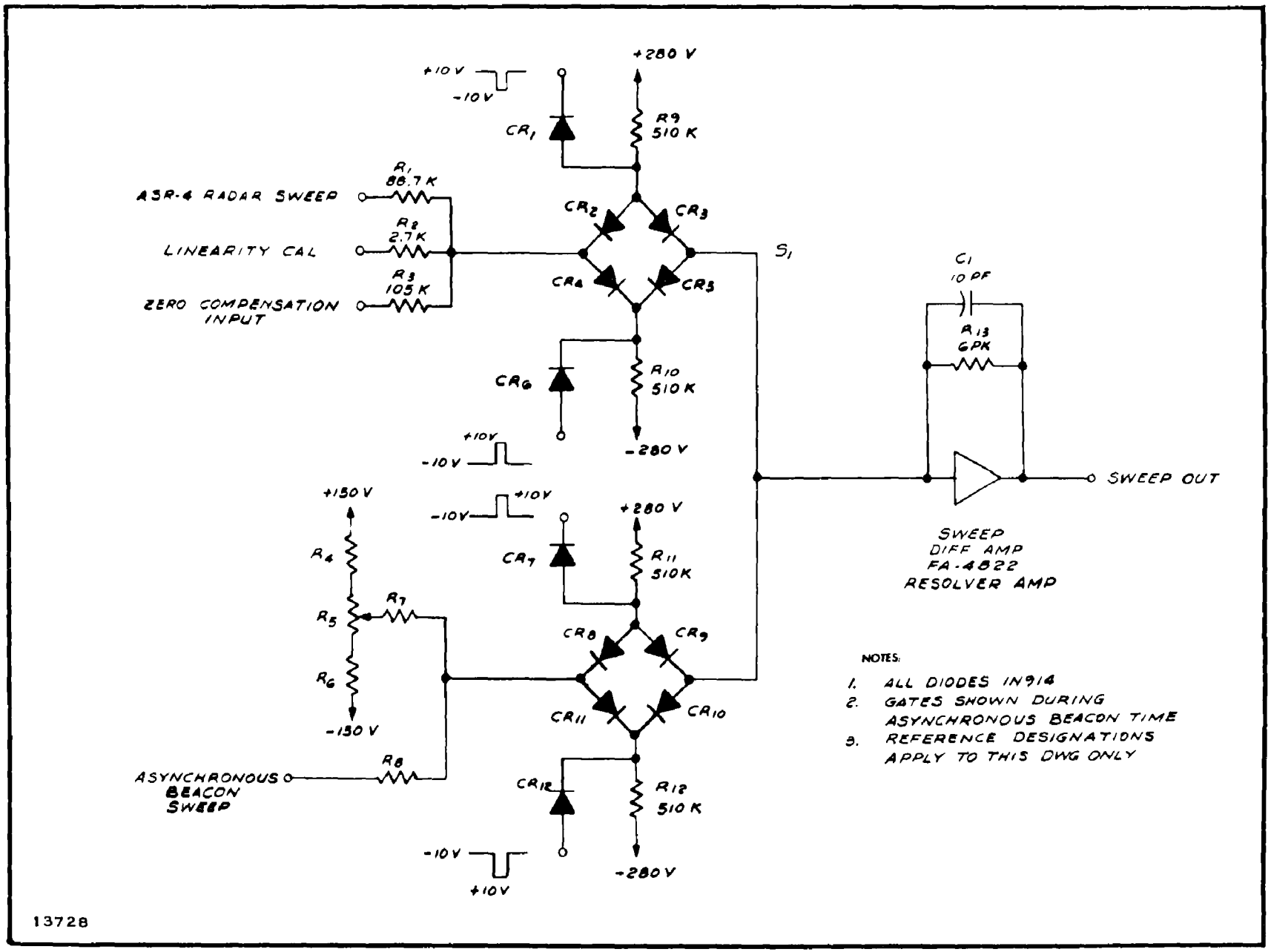

Figure 11. Asynchronous Beacon Sweep Time Share Circuits Schematic Diagram

6. Time Shared Clamp Trigger.

If a clamp trigger occurs during asynchronous beacon time, or if the clamp trigger resets the asynchronous beacon time share gate generator, the clamp trigger is inhibited. If, however, the clamp trigger occurs during normal radar time it must be passed to the ppi gate generator.

The positive asynchronous beacon time share and reset gate is taken from the output of OR circuit Q21 and Q23, inverted and amplified by Q34, and applied to AND circuit Q27. The clamp trigger is also applied to Q27. Thus, a clamp trigger will only be passed if it occurs between 25 microseconds after asynchronous beacon time and the start of the next asynchronous beacon time.

7. Time Shared Deadtime Trigger.

A deadtime trigger is required at the unblanking gate generator and ppi decenter unit either at the start of asynchronous beacon time or when there is a normal ASR-4 radar deadtime trigger; since the asynchronous beacon pretrigger can range between 5 volts and 50 volts, and the deadtime trigger must be at least 40 volts, it is necessary that circuitry must include provisions for possibly raising the amplitude of the beacon pretrigger.

The necessary trigger level is obtained by coupling the positive asynchronous beacon time share gate through emitter follower Q22 to differentiator R55 and C24. The positive trigger output is fed to OR circuit Q14 and is ORed with the ASR-4 deadtime trigger.

8. Time Shared Cursor Trigger.

A cursor trigger output is required if a normal cursor trigger occurs during ASR-4 time. There should also be a cursor trigger output at the end of asynchronous beacon time if the end of asynchronous beacon time occurs after a normal ASR-4 cursor trigger and before an ASR-4 deadtime trigger.

A bistable multivibrator Q4 and Q6 with input emitter follower limiters Q2 and Q8, which is identical to the asynchronous beacon gate generator, is used as a cursor trigger register. The collector of Q6 approaches +60 volts between ASR-4 cursor triggers and ASR-4 deadtime triggers and -20 volts at all other times. The gate is coupled to the collector of AND circuit Q11 through emitter follower Q9. A trigger is generated by coupling the negative asynchronous beacon time share gate through emitter follower Q10 to differentiator R29 and C13. The positive trigger thus generated occurs at the end of asynchronous beacon time and is applied to the base of AND circuit Q11.

The negative asynchronous beacon time share gate from the output of Q10 is coupled through emitter follower Q12 to the collector of another AND circuit Q13. The normal ASR-4 cursor trigger is applied to the base of the same AND circuit and the outputs of both AND circuits are ORed through the action of common emitter resistor R30. The time shared cursor trigger is fed from R30 to the unblanking gate generator and ppi decenter unit.

D. Status of Asynchronous Beacon Modification.

The initial detail design of the time share logic has been accomplished. Working breadboards of the time share logic are now being evaluated. The design is approximatly 75 percent complete with the remaining work being system evaluation and interface details with Options 2, 4, and 5. Preliminary design of interface circuitry is underway.

The asynchronous beacon modification as a whole is approximately 50 percent complete with the majority of the remaining work to be done in the area of the modified sweep generator and servoamplifier. An ASR-4 servo-amplifier is on order and will be available September 1. No work has been started on the modified sweep generator.

IV. ALPHA-NUMERIC DISPLAY MODIFICATION

A. Objective.

Work performed under Options 4 and 5 of contract No. FA-WA-4178 shall include development of modifications to provide for generation and display of alpha-numeric and symbolic data. Alpha-numeric and symbolic data is to be displayed upon digital computer command with a minimum off-time of radar data. The computer derived data has first priority on the display system and is to be displayed as soon as it is received. The computer message format is binary coded, containing data which allows generation of positioning voltages, velocity vectors, direction of leaders, various types of bars, alpha-numerics, and symbols.

The objective of Option 4 is to design, fabricate and build the electronic equipment which accepts, decodes and converts the computer data, assumes control of the ASR-4 display system, and displays the data on the direct view storage tube.

B. Design Approach.

1. Digital.

A major block diagram for Options 4 and 5 is shown by Figure 12. Option 4 is shown by the common equipment data conversion unit (DCU) in the center of the figure. The inputs to the DCU are: (1) The computer derived data, (2) Message generator data formatted to be accepted by the DCU as if it were computer derived data, (3) Slew dot coordinates that are gated directly into coordinates D/A converters and therefore not processed, (4) Console interface lines which provide field select, quick look, offset length, vector time control, and range scale inputs, and (5) Radar deadtime triggers and a clock.

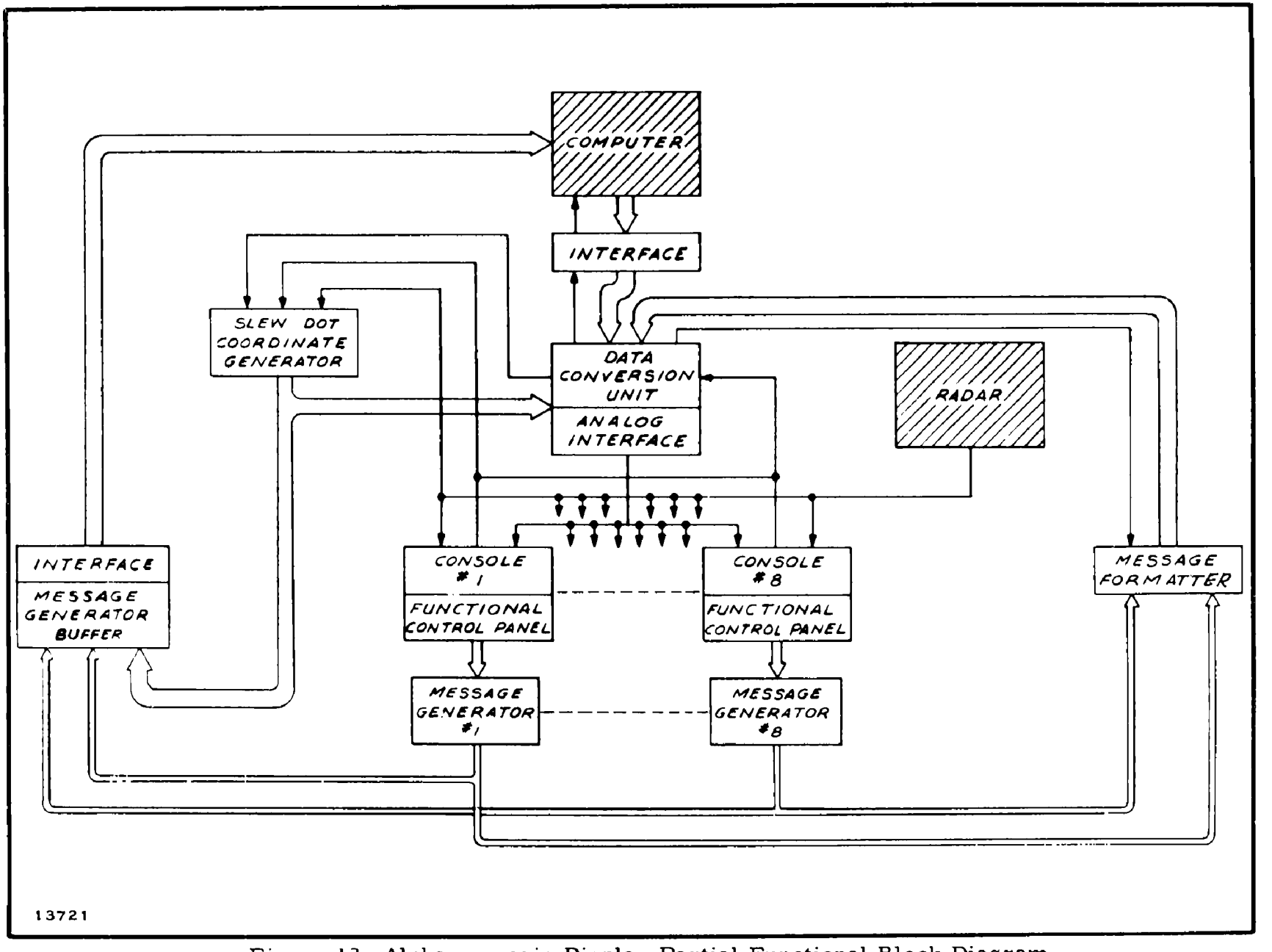

Figure 12. Alpha-numeric Display Partial Functional Block Diagram

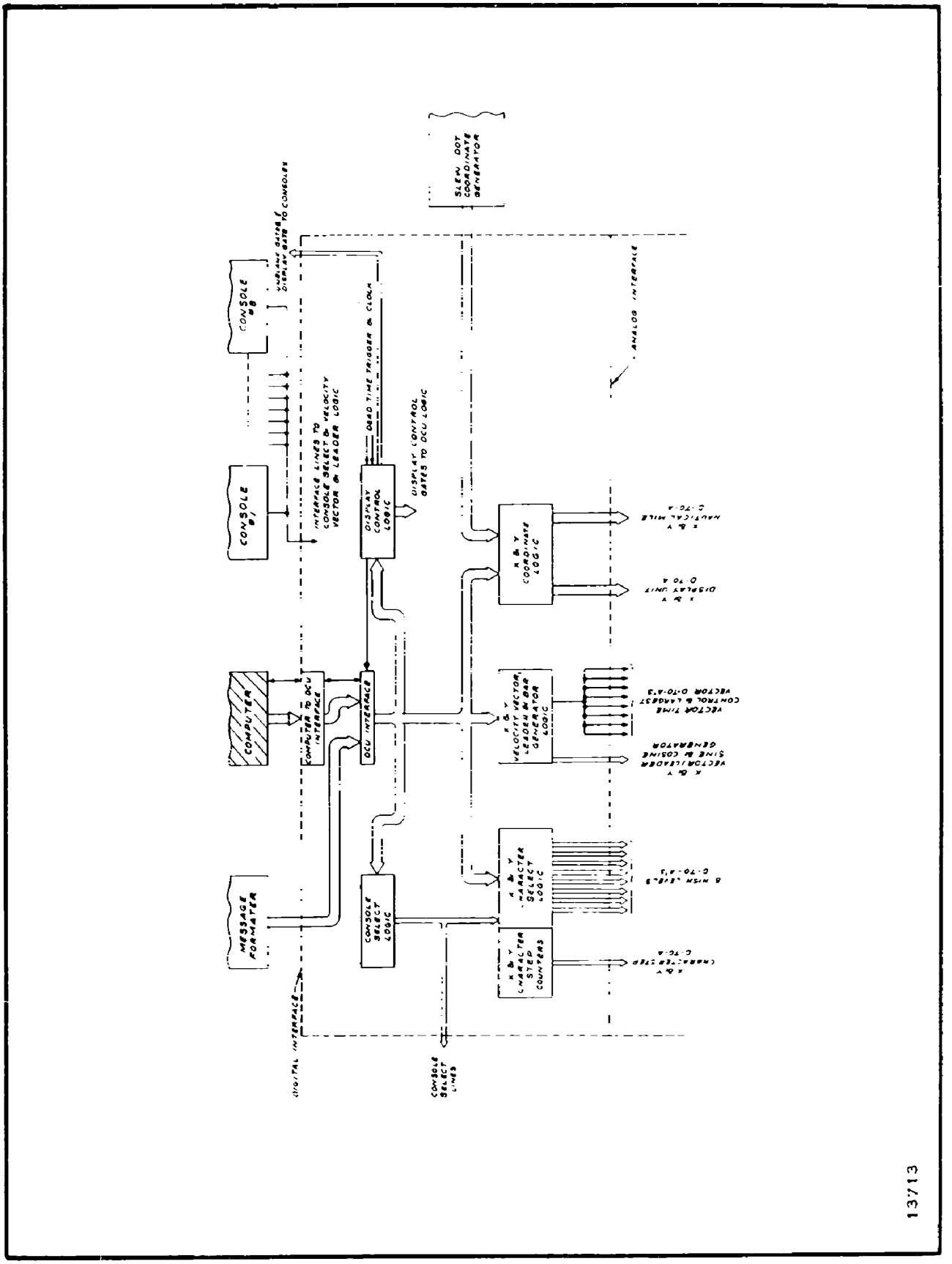

Figure 13. Data Conversion Unit Functional Block Diagram

The interface block above the DCU should be considered part of that unit but is shown separately to better illustrate the approach for displaying characters generated at the functional control panel.

The digital portions for Option 4 are shown in Figure 13. The analog interface is shown at the dashed line toward the bottom of the figure. Other interfaces shown are digital with the exception of some inputs from the consoles. The console select logic generates control gates for each console that instructs which inputs, alpha-numeric/radar display, that a given console should read. Console select gates are generated from instructions derived from the computer, functional control panel, or DCU itself. The console select logic is also used to control the high level D/A outputs to maintain the stroke writing position for all consoles that are not selected for alpha-numeric display.

The display control logic generates the basic timing and control terms to process the digital data for conversion to analog voltages. Unblank gates for stroke writing and characters are generated from the basic timing waveforms generated from the clock input.

Two interface registers, as shown by Figure 13, are incorporated to permit the processing of one data word while another is being requested and to permit the interfacing of characters generated by the functional control panel.

The basic DCU alpha-numeric/radar display cycle consists of the equivalent of two radar sweep times for alpha-numerics followed by two radar sweep times for radar and slew dot during radar deadtime. Timing for the alpha-numeric display is derived from two counters that are synchronized with the radar sweeps every fourth radar dead time trigger. The counter logic diagram and waveforms are shown by Figures 14 and 15, respectively. Figure 15 depicts the basic cycle as eight display words each consisting of eight time pulses of 50 microseconds duration (the time to print one character). The counters can advance to the condition of display word 8, time pulse 8, when it is forced to wait for the next deadtime trigger before continuing on to the next cycle.

Display word 1 through 4 is reserved for the display of alpha-numeric tags and functional control panel characters.

Display word 5 through 8 is reserved for radar, slew dot, and the processing of instructions from the computer.

The essential interface requirements for data transfer from the computer are that (1) when the first valid instruction word is transferred upon request from the DCU, a new instruction word will not be requested until the display timing (word and time) coincides with the time selected to process the first instruction word and (2) thereafter instruction words and data words shall be capable of being requested and received at the rate of one every 150 microseconds until the end of format (EOF) character is decoded. This is continued until the end of transmission (EOT) character appears in a format.

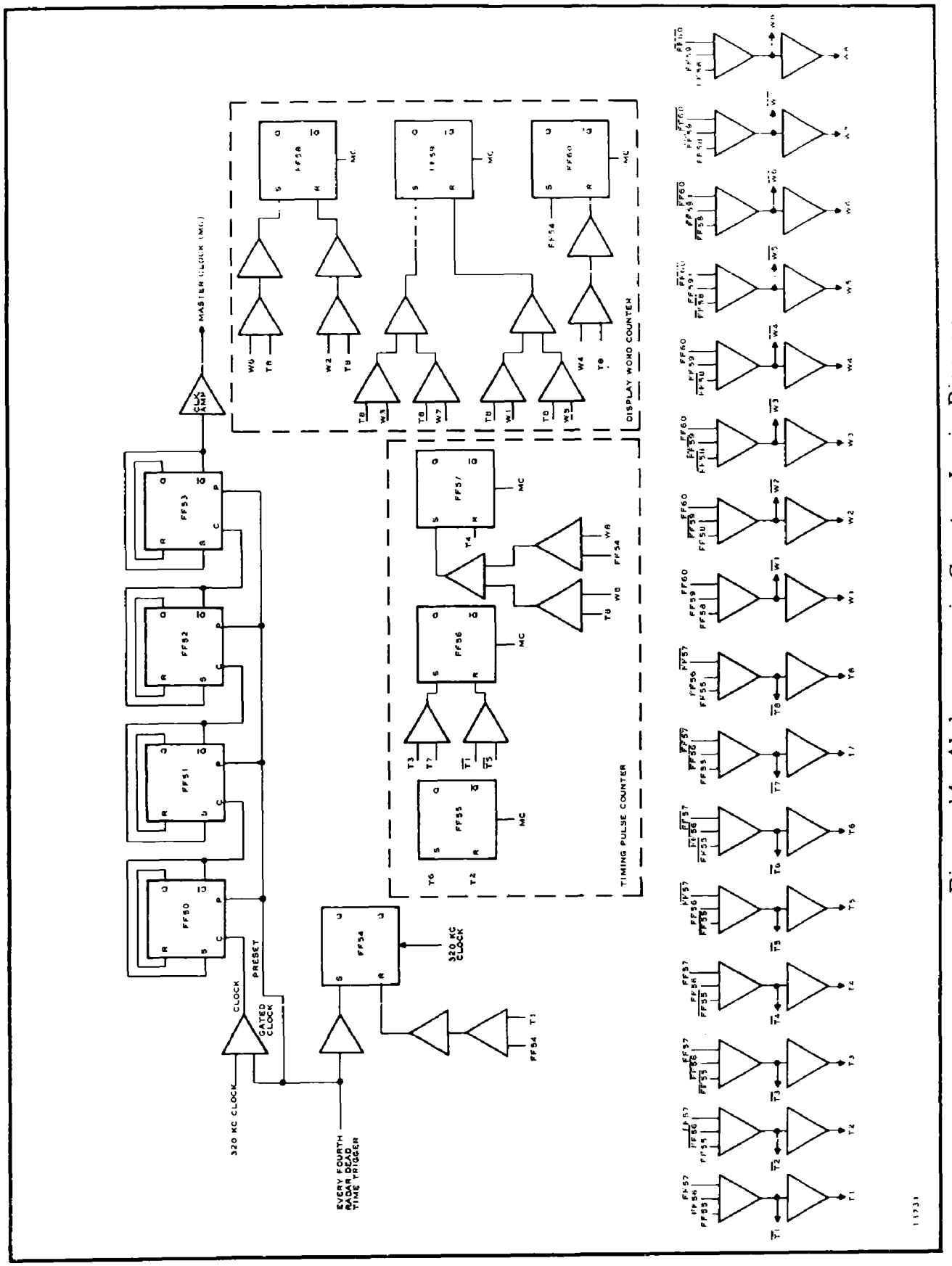

Figure 14. Alpha-numeric Counter Logic Diagram

Table I lists the DCU organization as related to the basic timing pulses shown in Figure 15.

2. Analog.

Figure 16 is a block diagram of the analog portions of Option 4.

The data conversion unit (see Design Approach, Digital), decodes the computer message and presents the digital information to the proper digital-to-analog converter.

a. Vector and Leader Generator.-The vector and leader generator shall generate ramp voltages of the appropriate magnitude and polarity as specified in the input digital message, to write vectors and leaders. All vectors and leaders will be written at a constant speed, thus avoiding any necessity for intensity compensation.

A beam writing speed of 50, 000 inches per second has been selected as a design objective. The beam writing speed is directly proportional to the rate of change of deflection voltage. The net deflection voltage will be the vector sum of the X and Y coordinate ramp voltages. The slope of the net deflection voltage will be a function of the beam writing speed and the deflection system characteristics. Therefore, it is necessary to regulate the X and Y coordinate ramp voltages in such a manner that the vector sum of their slopes shall remain constant.

To accomplish this end, a constant writing speed circuit has been incorporated into the vector and leader generator. The analog portion of the vector and leader generator is shown in Figure 17.

The digital inputs to the vector and leader generator consist of five bits plus sign for each coordinate voltage. The digital data, relating to vector or leader magnitude and orientation, determines the values of the gains K_x and K_y of the D/A converters. K_x and K_y have a maximum value of unit y. The D/A converter outputs, e_x and e_y, are presented to the inputs of the X and Y coordinate ramp generators. The ramp generators are high gain operational amplifiers with capacitive feedback. During the period of ramp generation, e_x and e_y will exist as dc voltage levels.

The magnitude of e_x and e_y will determine the slope of their respective ramp functions. The slope of the net ramp function is directly proportional to the vector sum of the slopes of the X and Y coordinate ramp deflection voltages. Thus to maintain a constant beam writing speed, it is necessary to regulate e_x and e_y in such a manner that their vector sum remains constant. The regulation of e_x and e_y is accomplished by summing the analog squares of e_x and e_y with a negative bias supply at the input terminal of an operational amplifier (A_1). Thus, the slope of the net deflection voltage is determined by the amplitude of the bias supply and the vector sum of e_x and e_y

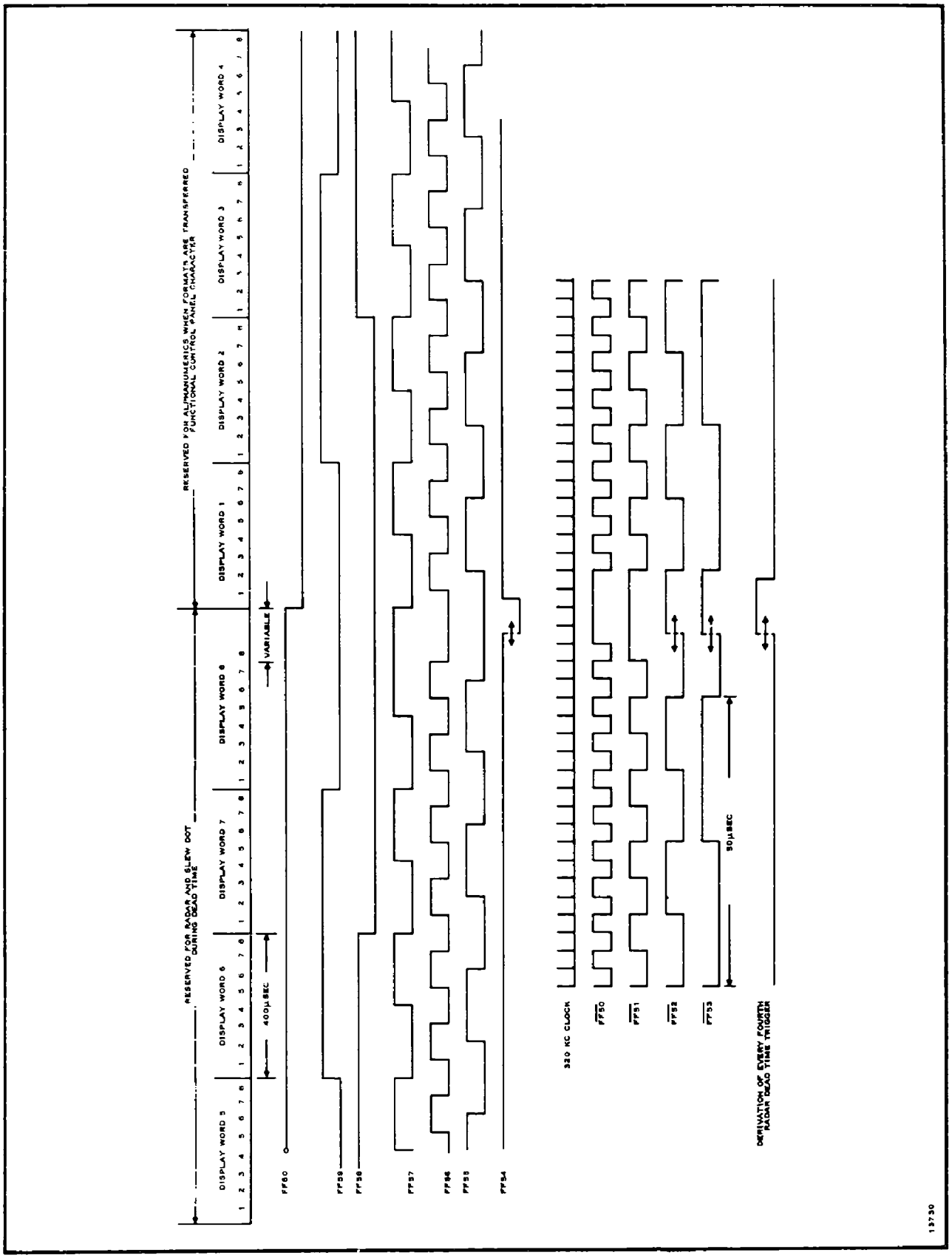

Figure 15. Alpha-numeric Counter Timing Diagram

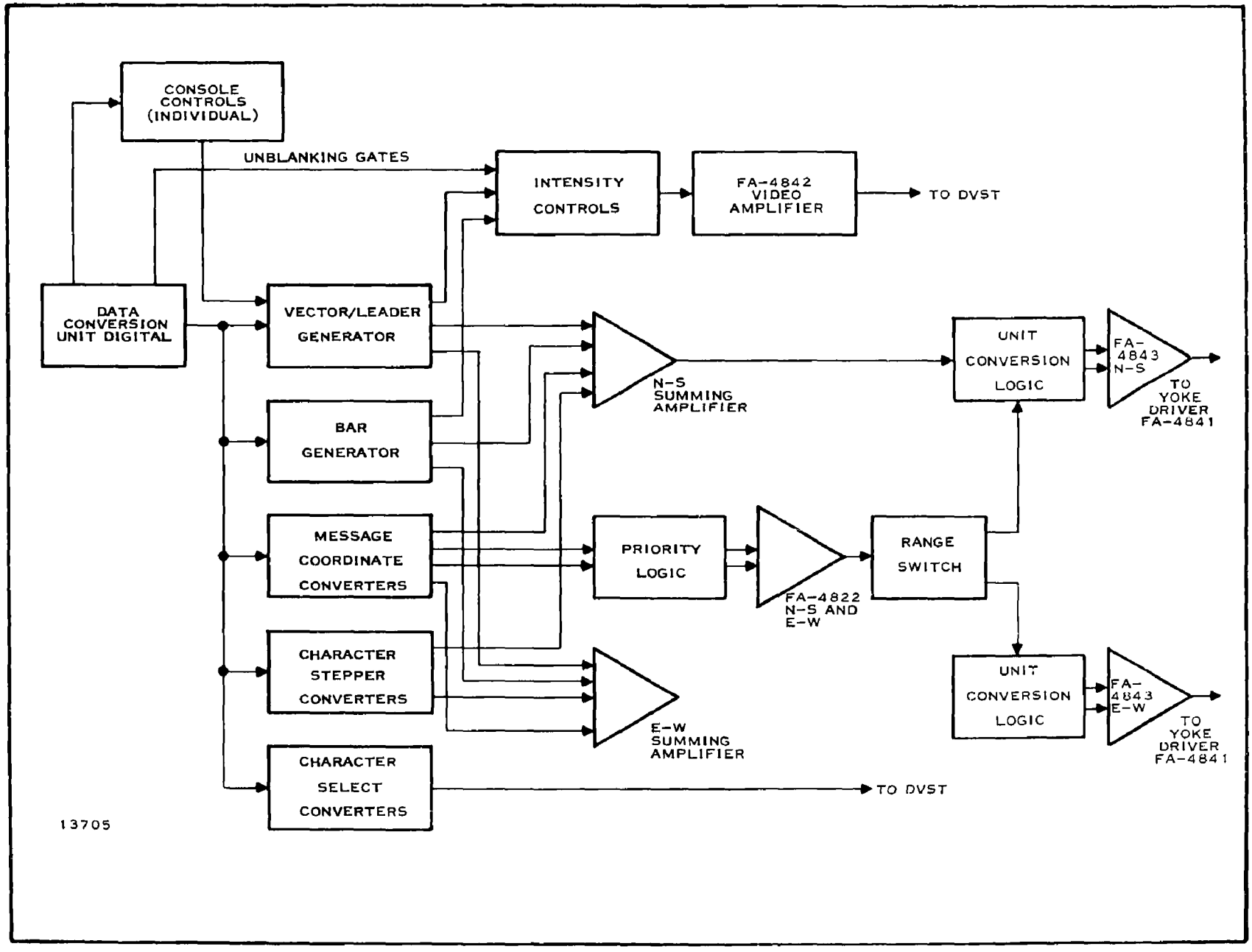

Figure 16. Alpha-numeric Display Functional Block Diagram

Table I. Data Conversion Unit Organization

DISPLAY WORD 7 TIME 1 –	SET INSTRUCTION F/F, STORE ADDRESS, COORDINATE UNITS AND FIELD SELECTS, REQUEST NEW INSTRUCTION WORD
DISPLAY WORD 7 TIME 2 –	UNUSED
DISPLAY WORD 7 TIME 3 –	STORE NEW INSTRUCTION WORD
DISPLAY WORD 7 TIME 4 –	STORE X-COORDINATE, REQUEST NEW INSTRUCTION WORD
DISPLAY WORD 7 TIME 5 –	UNUSED
DISPLAY WORD 7 TIME 6 –	STORE NEW INSTRUCTION WORD
DISPLAY WORD 7 TIME 7 –	STORE Y-COORDINATE, REQUEST NEW INSTRUCTION WORD
DISPLAY WORD 7 TIME 8 –	UNUSED
DISPLAY WORD 8 TIME 1 –	STORE NEW INSTRUCTION WORD
DISPLAY WORD 8 TIME 2 –	STORE X-VECTOR, STORE Y-VECTOR, STORE VECTOR TIME CONTROL INSTRUCTION, REQUEST NEW INSTRUCTION WORD
DISPLAY WORD 8 TIME 3 –	SCALE VECTOR-VECTOR SIZE COMPARISON
DISPLAY WORD 8 TIME 4 –	SCALE VECTOR, STORE LAST INSTRUCTION WORD
DISPLAY WORD 8 TIME 5 –	STORE SYMBOL, OFFSET INSTRUCTIONS, BAR INSTRUCTIONS REQUEST FIRST DATA WORD
DISPLAY WORD 8 TIME 6 –	SCALE VECTOR
DISPLAY WORD 8 TIME 7 –	STORE FIRST DATA WORD, GATE COORDINATE D-TO-A'S RESET INSTRUCTION F/F, SET ALPHANUMERIC DISPLAY F/F
DISPLAY WORD 8 TIME 8 –	WAIT FOR RADAR DEAD TIME TRIGGER RESET-OTHERWISE UNUSED
DISPLAY WORD 1 TIME 1 –	GATE CONSOLE SELECT LINES, GATE HIGH LEVEL D-TO-A'S, START ALPHANUMERIC DISPLAY GATE GENERATOR UNBLANK GATE FOR SYMBOL, GATE VECTOR/LEADER D-TO-A'S
DISPLAY WORD 1 TIME 2 –	GENERATE START OF VECTOR UNBLANK
DISPLAY WORD 1 TIME 3 –	UNUSED-VECTOR WRITING PERIOD
DISPLAY WORD 1 TIME 4 –	UNUSED-VECTOR WRITING PERIOD
DISPLAY WORD 1 TIME 5 –	VECTOR WRITING PERIOD AND GATE LEADER TO VECTOR/LEADER D-TO-A'S

Table I. Data Conversion Unit Organization (Continued)

DISPLAY WORD 1 TIME 6 – LEADER WRITE PERIOD–GENERATE LEADER UNBLANK

DISPLAY WORD 1 TIME 7 – UPPER BAR WRITE PERIOD–GENERATE BAR UNBLANK

DISPLAY WORD 1 TIME 8 – LOWER BAR WRITE PERIOD–GENERATE BAR UNBLANK

DISPLAY WORD 2 TIME 1 – DISPLAY CHARACTER NO. 1 REQUEST NEW DATA WORD

DISPLAY WORD 2 TIME 2 – DISPLAY CHARACTER NO. 2

DISPLAY WORD 2 TIME 3 – DISPLAY CHARACTER NO. 3, STORE NEW DATA WORD

DISPLAY WORD 2 TIME 4 – DISPLAY CHARACTER NO. 4, REQUEST NEW DATA WORD

CHARACTER DISPLAY IS TERMINATED AT END OF FORMAT CHARACTER

DISPLAY WORD 4 TIME 8 – DISPLAY CHARACTER NO. 24

DISPLAY WORD 5 TIME 1 – RELEASE DISPLAY TO SLEW DOT ON NEXT DEAD TIME TRIGGER AND RADAR ON NEXT SWEEP GATE, REQUEST NEW INSTRUCTION WORD

DISPLAY WORD 5 TIME 2 – SLEW DOT ON DEAD TIME TRIGGER AND RADAR DISPLAY

DISPLAY WORD 6 TIME 8 – STORE FIRST INSTRUCTION WORD IF RECEIVED

DISPLAY WORD 7 TIME 1 – SET INSTRUCTION F/F IF NEW INSTRUCTION WORD WAS STORED AND CONTINUE RADAR DISPLAY

DISPLAY WORD 8 TIME 7 – SAME AS DISPLAY WORD 8 TIME 7

DISPLAY WORD 8 TIME 8 – WAIT FOR RADAR DEAD TIME TRIGGER OTHERWISE UNUSED

NOTE:
CHARACTERS FROM FUNCTIONAL CONTROL PANELS ARE FORMATED AS A COMPUTER MESSAGE AND PROCESSED IN A MANNER IDENTICAL TO A COMPUTER DERIVED FORMAT AS TABULATED ABOVE

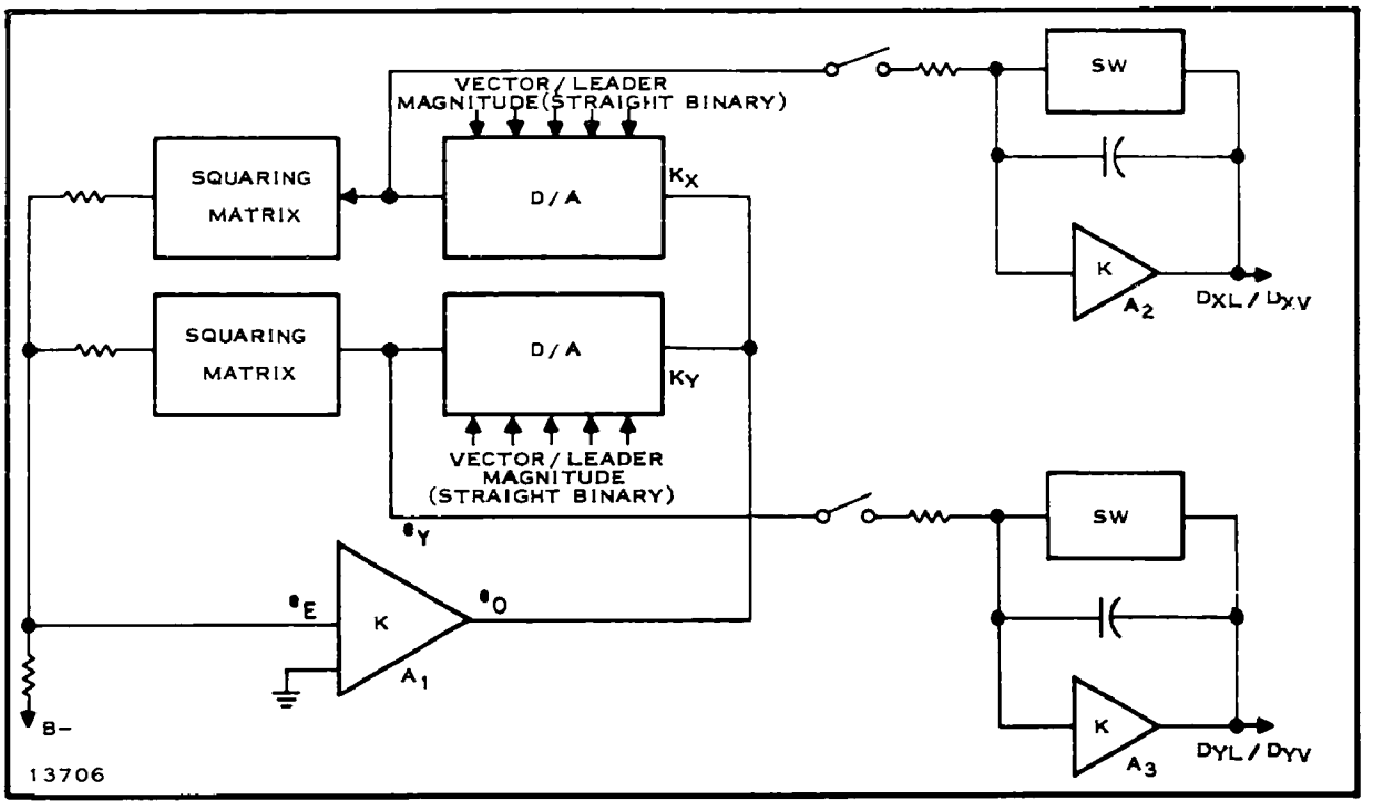

Figure 17. Vector/Leader Generator Functional Block Diagram

is forced to this value by the action of the operational amplifier. In summary, the vector sum of e_x and e_y is determined by the magnitude of the bias supply, while the relationship of e_x with respect to e_y is determined by the digitally selected values of gain, K_x and K_y.

Solid-state switches are placed in the feedback loops of the ramp generators to provide necessary control over ramp start and stop voltage levels. Switches in the feedback loops are also used to maintain voltage levels at the conclusion of leader writing. These voltage levels are maintained as a reference voltage during the print time of the alpha-numerics.

The X and Y coordinate voltages will always have positive polarity. Thus, the sign bits in the input digital message are used, when required, to initiate appropriate switching to route the ramp voltages through inverting unity-gain amplifiers.

b. Bar Generator. - The bar generator, shown in Figure 18, produces a standard length ramp output (7 characters wide) which is summed in the east-west summing amplifier. Control of the ramp is accomplished by the digital inputs. A signal (BW) activates BWFF which opens switch S1, turns on gate G1, allows the ramp to be generated. Simultaneously, BW turns on gate G3 which adds an incremental voltage to the north-south summing amplifier. This incremental voltage positions the bar above the first

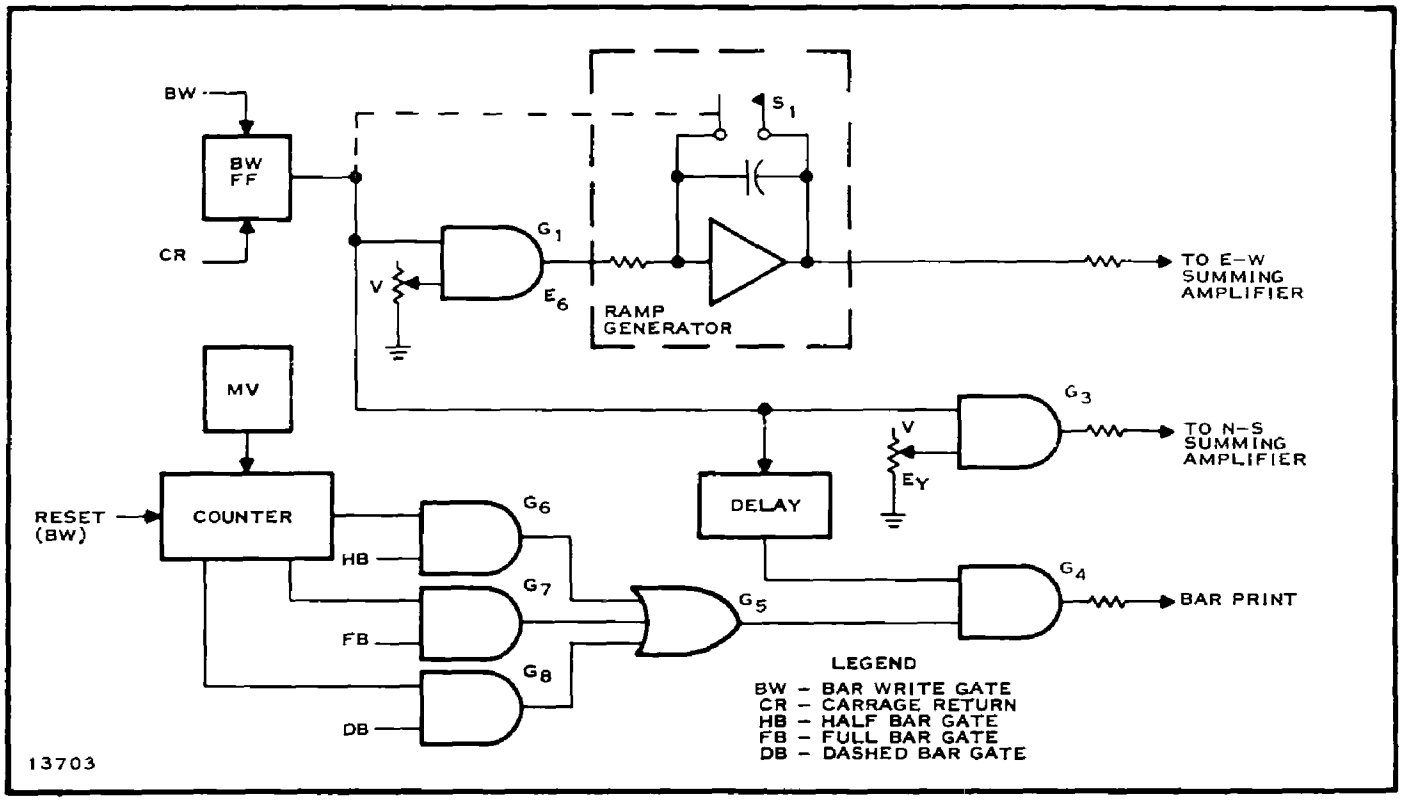

Figure 18. Bar Generator and Print Gate Block Diagram

line of characters in the "tag." Unblanking signals are generated from a counter which is reset by BW. Outputs of the counter are of the proper duration so that, with proper gating signals decoded from the basic DCU timing, either a half, full, or dashed bar is printed. A signal (CR) from the digital section of the DCU resets BWFF which returns the ramp to zero and inhibits G3 and G4.

c. Message Coordinate Converters. - There are two separate sets of message coordinate converters, one for nautical miles (when the computer message is in radar coordinates) and one for display units. A set consists of one north-south and one east-west D/A converter. Inputs are straight binary, with ones, complement for negative numbers. Outputs are from +10 volts dc to -10 volts dc.

The output of the nautical mile converter is applied to Resolver Amplifier FA-4822. The output of the resolver amplifier is range switched and summed in PPI Decenter Time Share and Mixer FA-4843. When the computer message is in display units, the output of the converter is applied to FA-4843 on a separate input. When a "tag" is to be displayed, ASR inputs to the resolver amplifier are switched off and the message coordinates substituted. Figure 19 is a diagram of the summing point switching involved. The diode switches (1, 2, and 3) are controlled by priority logic (see Figure 20). A control signal (alpha-numeric gate) from the DCU will go true when a "tag" is to be displayed. The priority logic will apply control signals to turn off switches 1 and 2 and turn on switch 3. Simultaneously, the state of the display unit gate

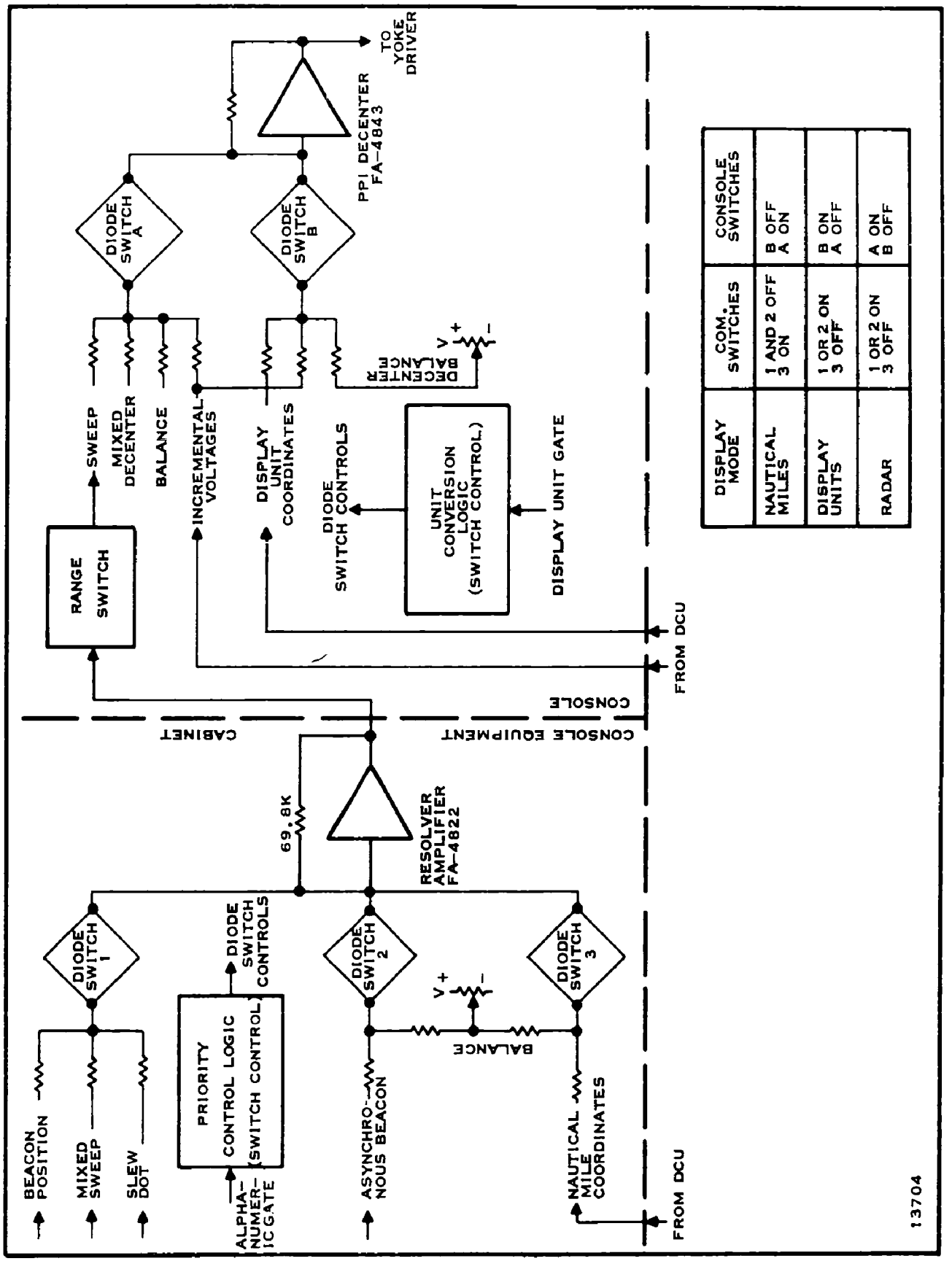

Figure 19. Interface Block Diagram

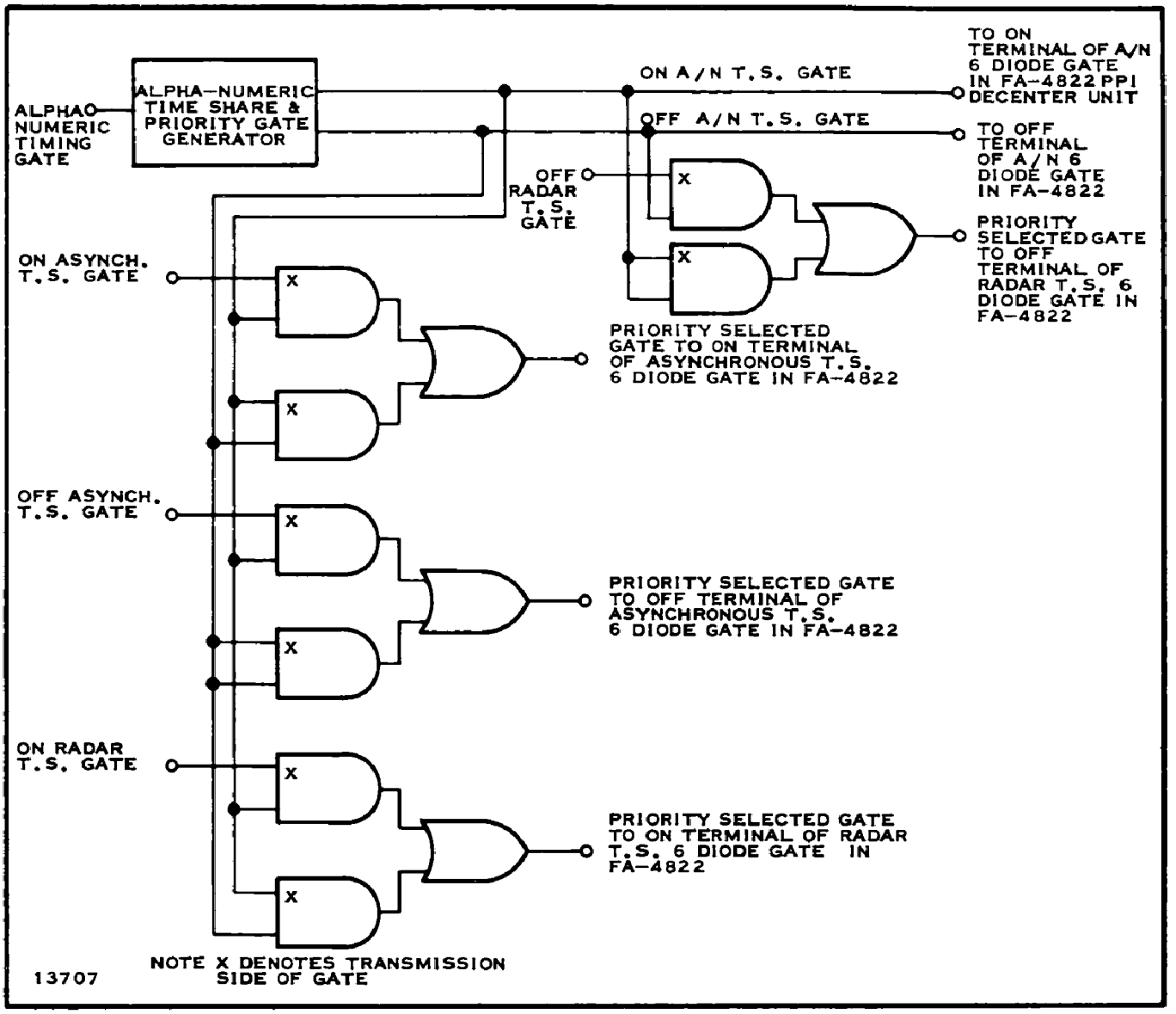

Figure 20. Alpha-numeric Priority and Time Share Logic Block Diagram

informs the unit conversion logic (see Figure 21) whether the message coordinates are in nautical miles or display units. If the message coordinates are in nautical miles, switches A and C will be turned on. If the message coordinates are in display units, switches A and C will be turned off and switch B turned on. Thus, nautical mile information is range-switched and decentered while display unit information is not.

d. Character Stepper Converters. - The character stepper converters provide incremental deflection voltages which position the alpha-numeric characters on the face of the DVST. The east-west converter adds a positive increment each time another character is to be displayed and is reset to zero by a carriage return character. The carriage return character causes

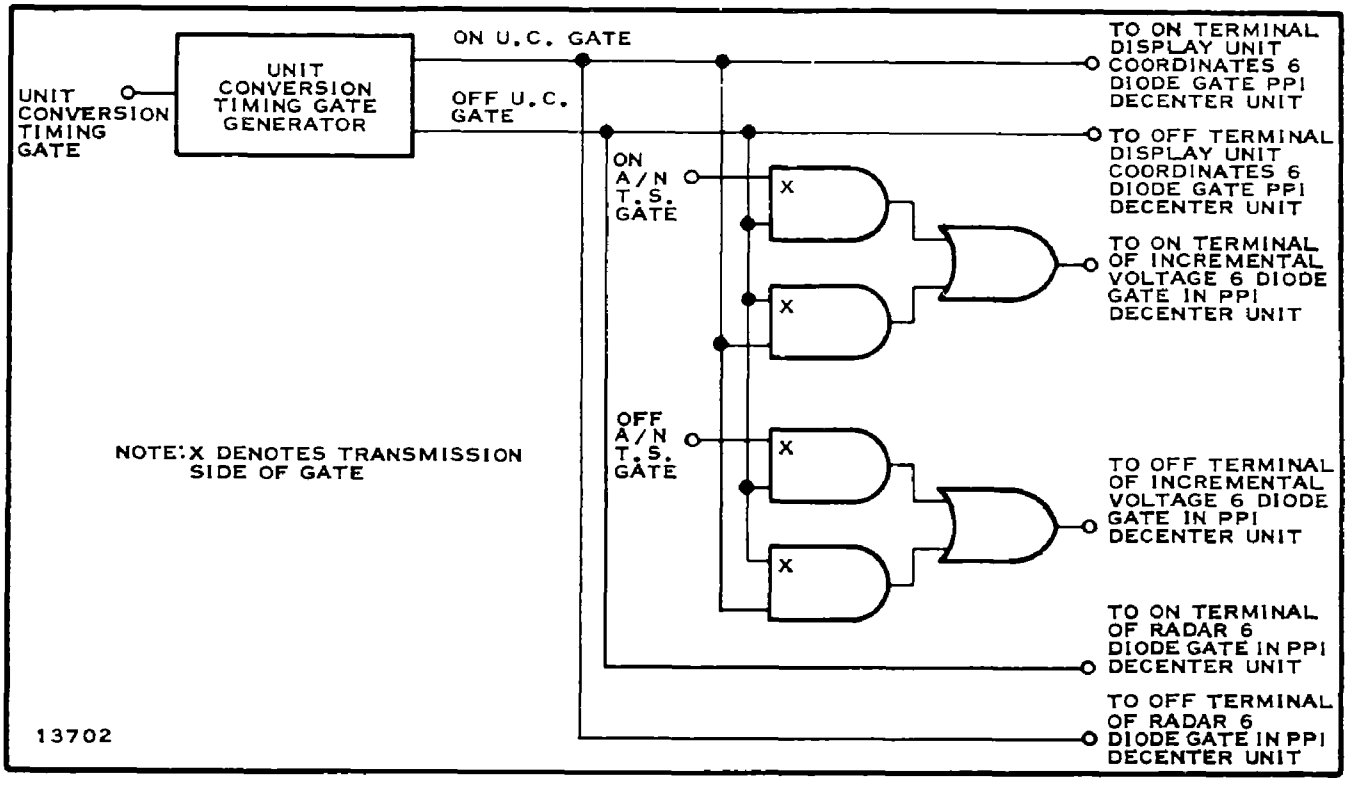

Figure 21. Unit Conversion Logic Block Diagram

the north-south converter to step to a more negative voltage which positions the next line of characters on the face of the DVST.

e. High-Voltage D/A Converter. - The purpose of the high-voltage D/A converter is to drive the electrostatic deflection plates of a direct-view storage tube. The electrostatic plates position the electron beam to the characters, located on the matrix, defined in the digital input message.

Breakdown characteristics limit the available output voltage when transistors are used in D/A converters. However, a hybrid tube-transistor circuit can be used to obtain a large analog voltage swing from an input of parallel bits of digital information. The block diagram in Figure 22 illustrates the bit-current summing technique used in the converter.

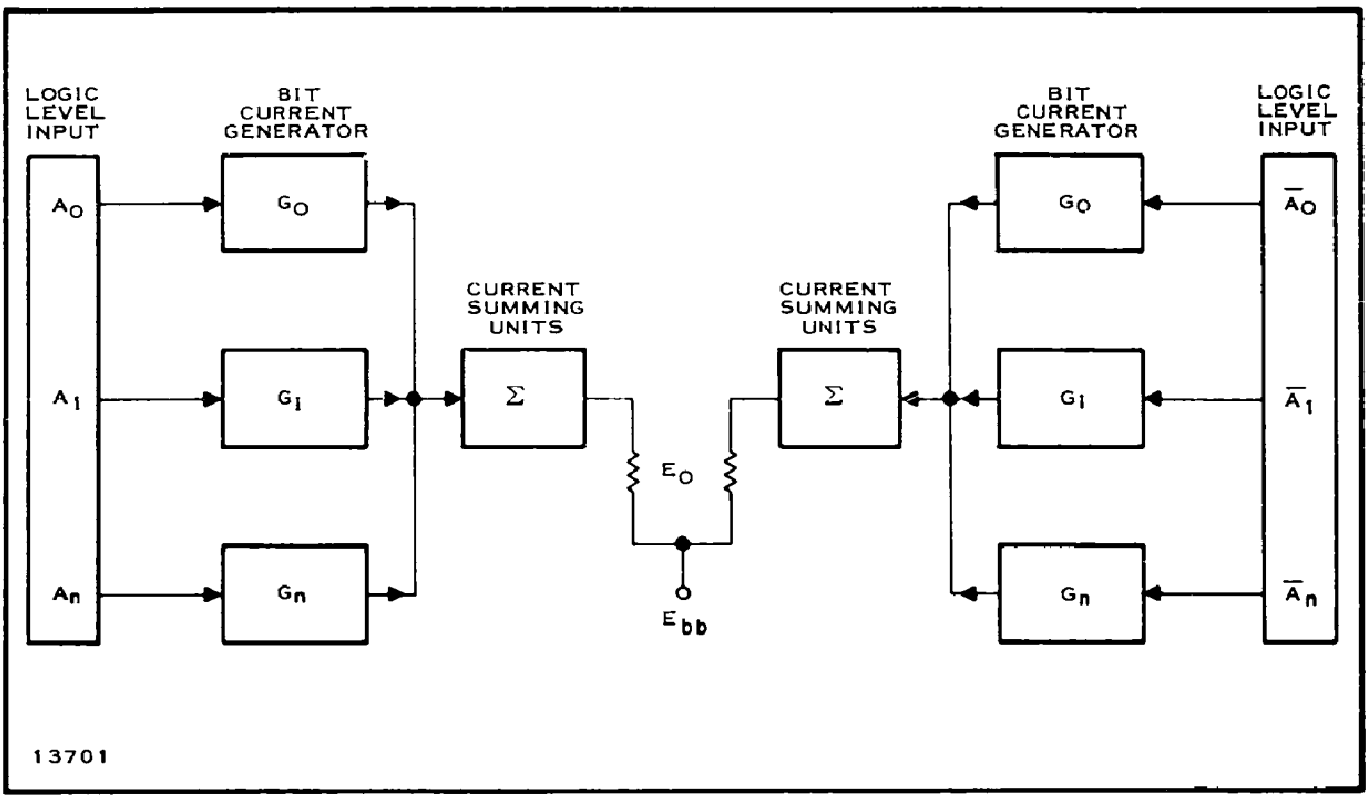

Figure 22. Bit Summing Logic Block Diagram

Figure 23 shows a simple schematic of one-half of the D/A converter. The circuit enclosed in the dashed lines in a compound-connected circuit that tends to maintain the emitter of Q1 at a constant potential (close to V1). The emitter current of Q1 will be relatively small for a large range of currents through the emitter of Q2. Thus, the potential at the emitter of Q1 will be relatively unchanged for large emitter-changes in Q2.

The relatively constant voltage at the emitter of Q1 makes it suitable for use as a current summing point. Because the collector-emitter breakdown potential of most transistors is too low to provide a wide output voltage swing, the summed currents are fed into a vacuum-tube grounded-grid amplifier.

The digital input data is fed into inverter inputs A_0, A_1, A_2, and A_3. The collector resistors of each inverter are binary-weighted. Each of the emitters is tied to V_1, which is very close to the emitter potential of Q1.

When any of the inverters are in the conduction state the potential across 2^nR_B (n = 0, 1, 2, and 3) is very nearly zero, and a negligible current will be contributed by this stage to the summing point. When any of the inverters are in the nonconduction state, the current contributed to the summing point, neglecting leakage, will be:

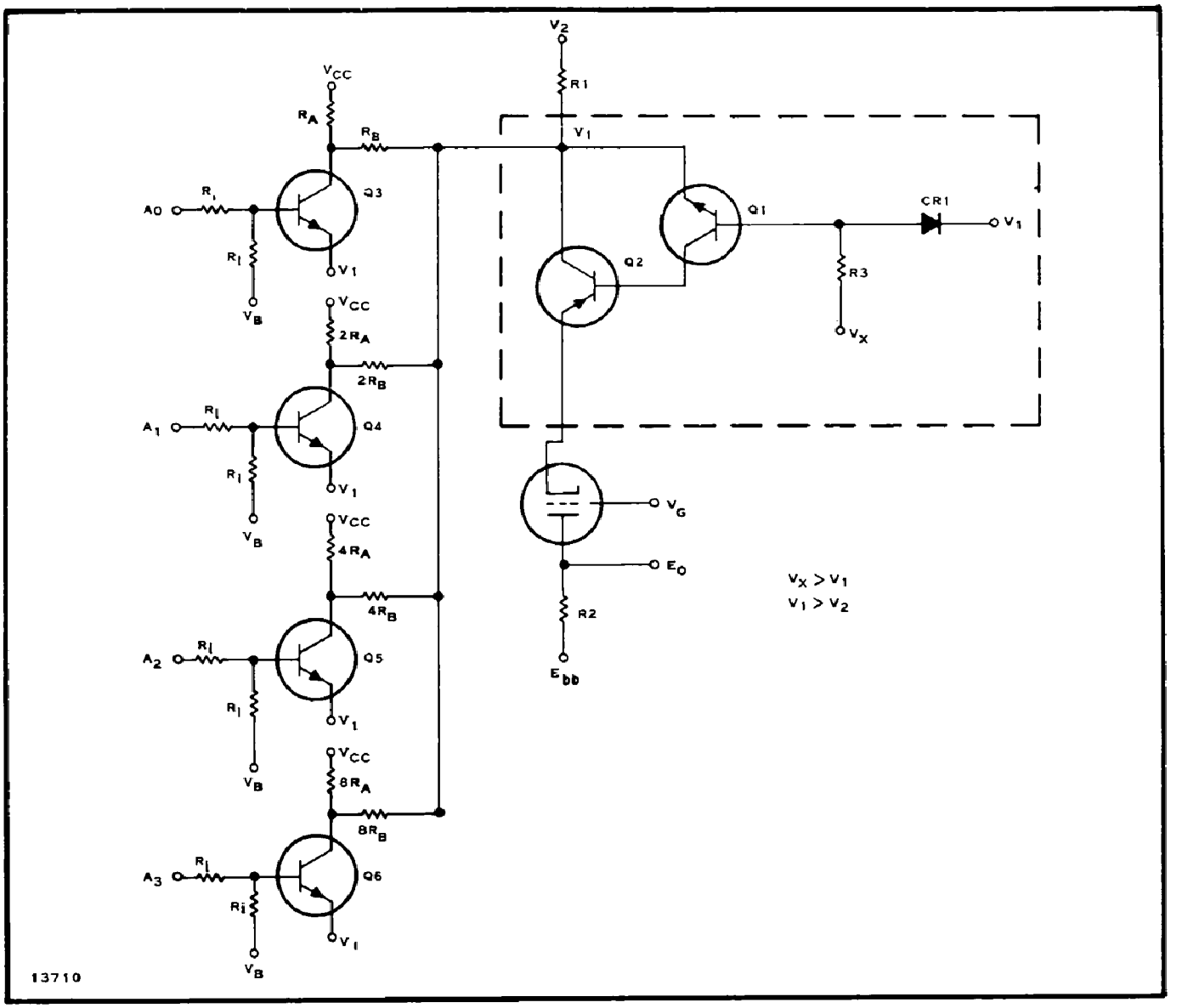

Figure 23. One Half of D/A Converter Partial Schematic Diagram

$$I_{vn} = \frac{V_{cc} - V_1}{(R_A + R_B)2^n}, \qquad (1)$$

where 2^n designates the binary weighting of any stage.

A bias current will always flow through R_1. Therefore, when all inverters are in the conduction state, the plate current is:

$$I_p = \frac{V_1 - V_2}{R_1}. \qquad (2)$$

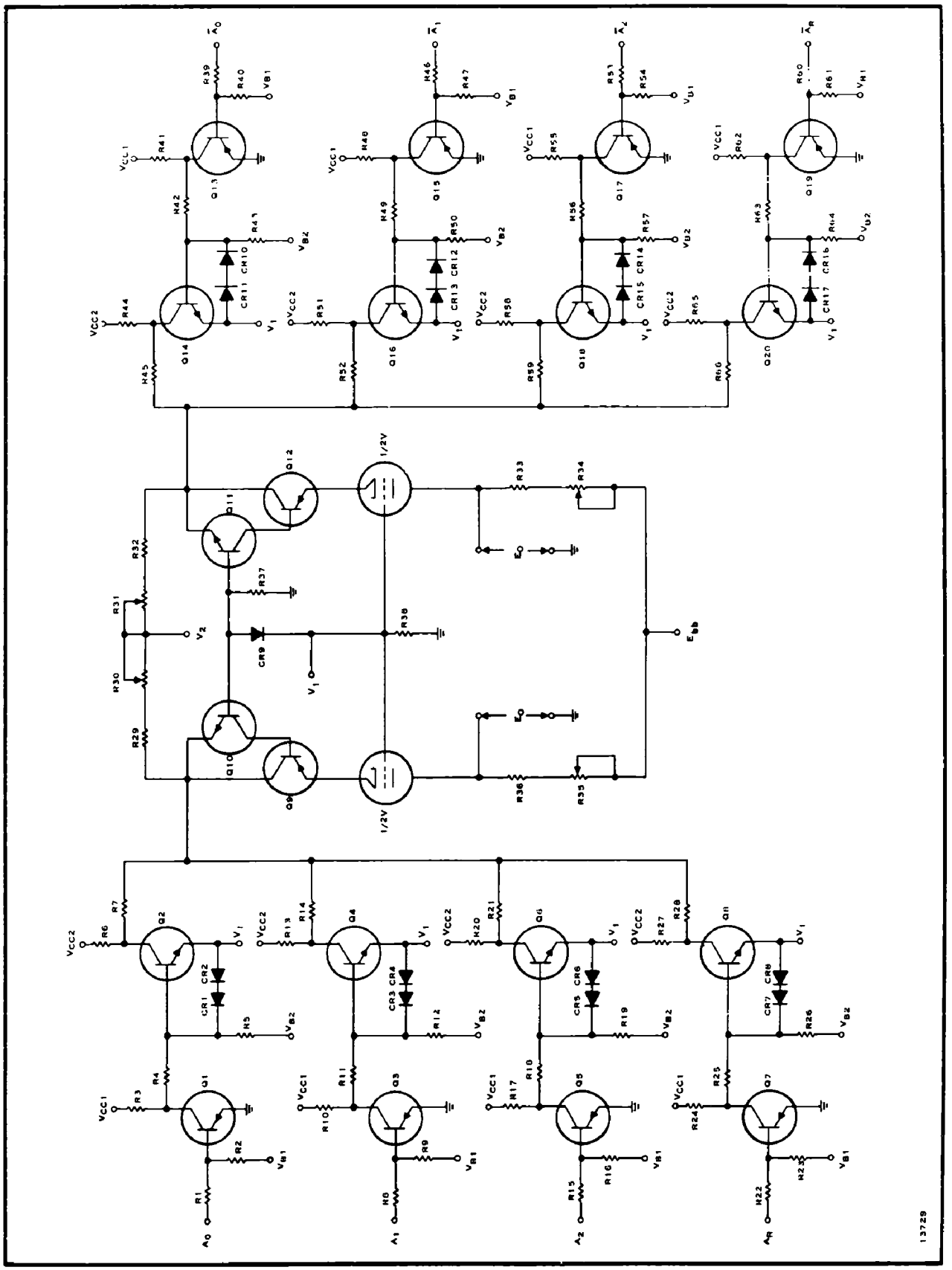

Figure 24. High Voltage D/A Converter Partial Schematic Diagram

Table II. Desired Digital Inputs Versus Analog Output Voltages

Input Code (Y Plates) X Plates			Output Voltages (Upper Y Plates) Right X Plates	Output Voltages (Lower Y Plates) Left X Plates
A_0	A_1	A_2		
0	0	1	170.5 volts	-60.5 volts
0	1	0	137.5 volts	-27.5 volts
0	1	1	104.5 volts	5.5 volts
1	0	0	71.5 volts	38.5 volts
1	0	1	38.5 volts	71.5 volts
1	1	0	5.5 volts	104.5 volts
1	1	1	-27.5 volts	137.5 volts
			-60.5 volts	170.5 volts
"ONE" on Radar Write-line			Upper and Lower Y Plates +55 volts	Right and Left X Plates +55 volts

Notes:
A. "ONE" refers to "logical one" which is 0 to 0.5 volt
B. "1" refers to "logical one" which is 0 to 0.5 volt
C. "0" refers to "logical zero" which is 3.8 to 6.0 volts
D. "ONE" on Radar Write-line positions the electron beam through an aperture in the center of the matrix.

This current will correspond to the highest plate current that the tube will conduct (and the lowest output voltages), since turning off any inverter will decrease the plate current by the amount in Equation (1) and consequently increase the output voltage.

The desired digital inputs versus the analog output voltages are given in Table II.

A schematic of the proposed High-Voltage D/A is shown in Figure 24.

f. Slew Dot Generator. - Figure 25 is a functional block diagram of the X channel of the slew dot generator. The Y channel is identical except that the analog switching matrix, mod 8 counter, decode gates, control logic, clock and clock gates will be common to both channels.

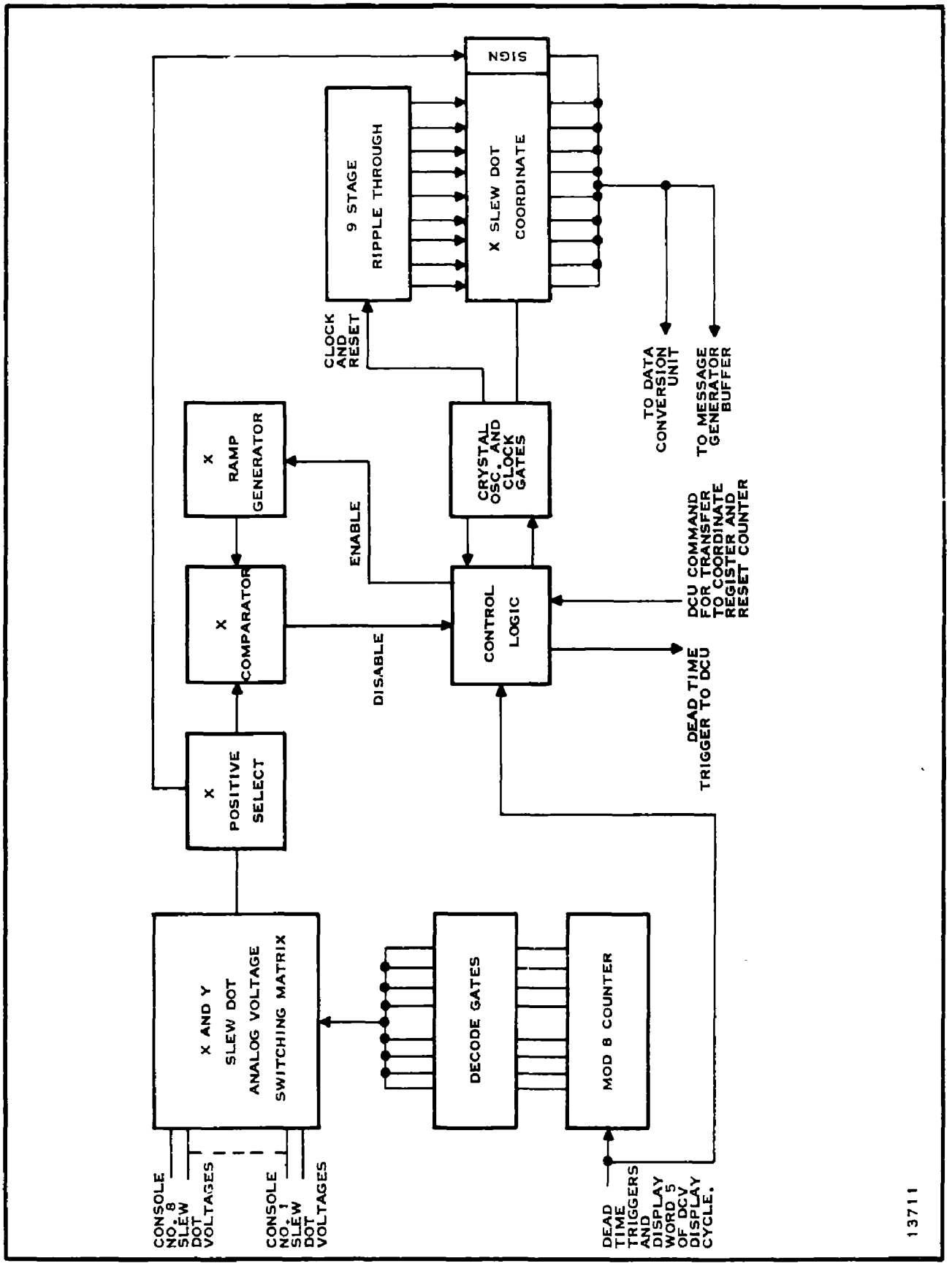

Figure 25. X Channel Slew Dot Coordinate Logic Functional Block Diagram

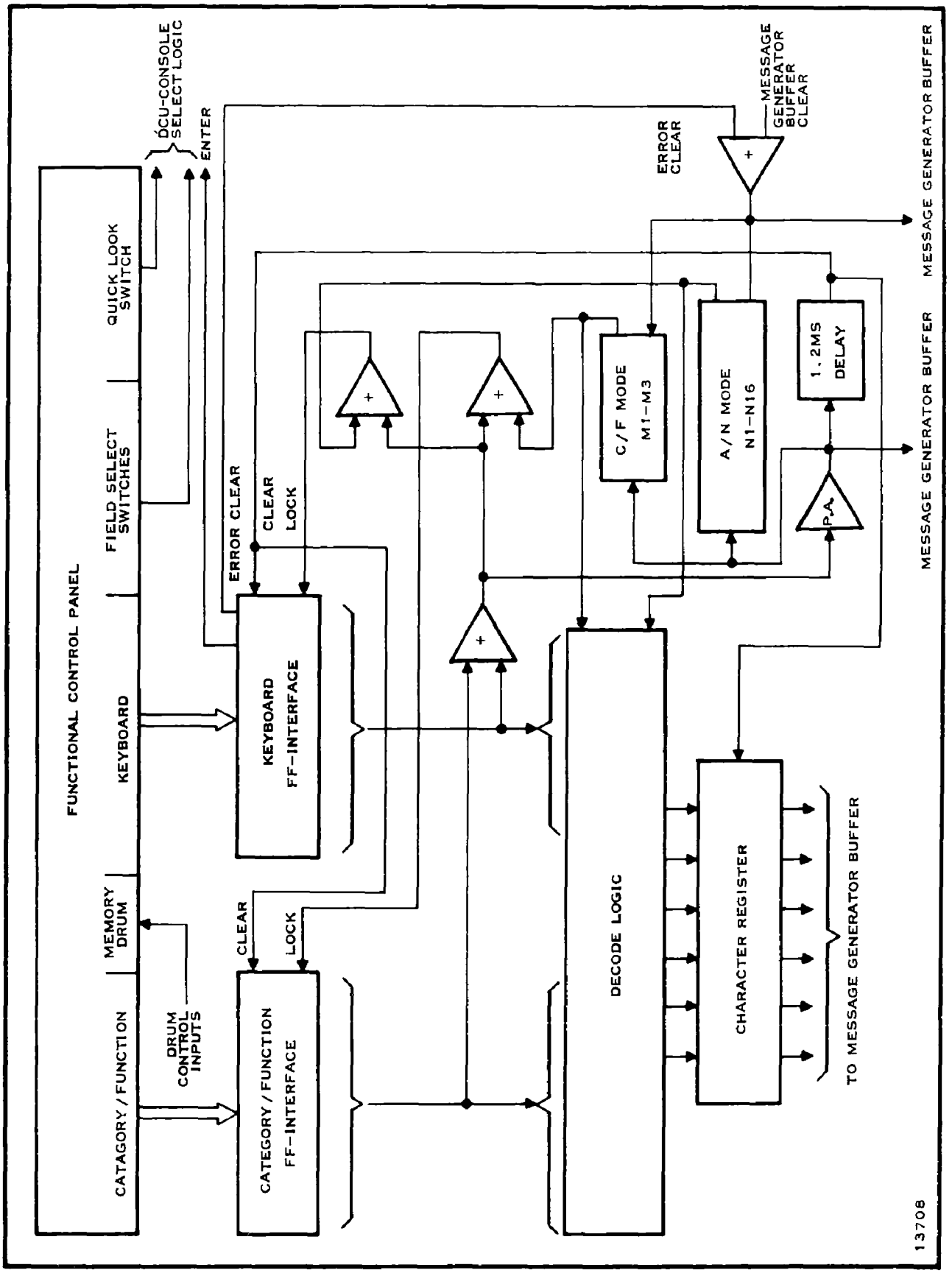

Figure 26. X Message Generator Separate Equipment Logic Functional Block Diagram

The mod 8 counter advances with every radar deadtime trigger (DTT). occurring during display word 5 (every fourth deadtime trigger) and each counter decode gate enables one pair of 8 console X and Y slew dot analog voltages. The analog voltages are applied to comparators via a positive select switch which eliminates the need to generate a bipolar ramp. The ramp generator is enabled by the control logic after the occurrence of an enabled DTT. After a short delay to eliminate ramp nonlinearities the control logic enables a clock gate which starts the 9 stage ripple through counter. The clock is disabled when the ramp output is equal to the slew dot voltage input. After sufficient time is allowed for converting the maximum slew dot voltage, the DCU commands that the contents of the counter be transferred to the slew dot coordinate register using the sign bit to determine whether the complemented or uncomplemented counter number should be transferred. The counter is then reset to start the next conversion. The result is that while one set of slew dot coordinates is being displayed or transferred to the buffer memory, the subsequent set of slew dot coordinates is being converted.

g. Message Generator. - The functional logic block diagram of the message generator is shown in Figure 26. The message generator is a completely asynchronous subsystem performing the man-to-machine interface. The characters generated in the message generator are stored in the message generator buffer common equipment for display and eventual entry into the computer.

The functional control panel contains the category/function switches, the category/function display drum, the keyboard for selecting alpha-numeric symbols, the field select switches for controlling which data in the display format is to be inhibited from display and the quick-look switch enabling a console operator to display the complete display formats intended for one of the other seven display consoles. The field select and quick-look outputs are interfaced with the display control unit .

The flip-flop interfaces between the functional control panel and the decode logic contain one flip-flop for each category/function and keyboard switch. A flip-flop is set true by the corresponding control panel switch provided the interface is not locked-out by the control logic. This electronic lock-out prevents the operator from incorrectly assembling a format and also prevents the loss of a character during the period the stored information is being read by the DCU.

The decode logic converts flip-flop interface data into six bit character codes and sets up the six bit output character register. The output character register presents the six bit character code to the message generator buffer.

The message generator timing is controlled by the category/function (C/F) mode counter and the alpha-numeric (A/N) mode counter. The C/F mode counter controls the decoding of the category and the

function, and locks-out the C/F flip-flop interface except when the category or function are to be selected. The A/N mode counter controls the decoding of A/N characters and locks-out the keyboard flip-flop interface except when A/N characters are to be selected.

The selection of a category or function or alpha-numeric at the proper time is detected in an OR gate and generates a lock-out signal to both flip-flops, advances the mode counters via a pulse amplifier, and feeds a pulse into a 1.2 millisecond delay circuit. After 1.2 milliseconds a clear signal is generated that clears the flip-flop interface and shifts the decoded character into the output character register. The new state of mode counter determines which (if either) of the interfaces is not locked and hence ready for the next character from the functional control panel switches. Both interfaces are locked if the message generator buffer is filled. The 1.2 millisecond delay between the selection of an input by the operator and the readout of the character code into the output register prevents a character from being discarded during the time the message generator buffer is being read into the DCU. 1.2 milliseconds is slightly greater than the maximum time required for the buffer readout of the A/N characters. No characters are read into the buffer during the time the buffer is being sampled by the DCU.

h. Message Generator Buffer. - The message generator buffer will provide the storage elements necessary to contain the eight separate messages composed by the console operators. Each message contains a maximum of seventeen 6-bit characters (category, function, and fifteen alpha-numeric characters). The minimum storage capacity required for eight console configurations is 816 storage elements. In addition there will be the necessary logic control elements for reading in and reading out the stored information. The readin and readout circuitry probably cannot be confirmed because the readin is asynchronous (at the speed of the operator) and the readout is at a rate compatible with the display control unit and the computer. Because of the high storage element count, some consideration will be given to magnetic core storage.

The message generator buffer outputs drive the buffer-to-computer formatter and the buffer-to-display formatter. The two formats required are shown in Tables III and IV.

C. Status of Alpha-Numeric Display Modification.

Since a hold order has been in effect on the portions of Options 4 and 5 related to the computer interface and message format, design work has been limited to general investigations of digital-to-analog interface, ASR-4 to modification 4 interface, character select and compensation converters, and generation and control of voltage ramps needed for display of vectors, leaders, and bars. Detail design has been performed on the feasibility of diode gate switching of operational amplifier summing points. Modification specifications are not yet definitized concerning computer interface and message format.

Table III. Message Format (Message Generator Buffer to Computer)

	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WORD NO. 1	CONSOLE BITS										SPARE							
WORD NO. 2	SPARE				FUNCTION*						CATEGORY*							
WORD NO. 3	SPARE				A/N NO. 2 *						A/N NO. 1*							
WORD NO. 4	SPARE				A/N NO. 4*						A/N NO. 3*							
WORD NO. 5	SPARE				A/N NO. 6*						A/N NO. 5*							
WORD NO. 6	SPARE				A/N NO. 8*						A/N NO. 7*							
WORD NO. 7	SPARE				A/N NO. 10*						A/N NO. 9*							
WORD NO. 8	SPARE				A/N NO. 12*						A/N NO. 11*							
WORD NO. 9	SPARE				A/N NO. 14*						A/N NO. 13*							
WORD NO. 10	SPARE				ALL ZERO CHARACTER						A/N NO. 15*							
WORD NO. 11	X COORDINATE OF SLEW DOT									LSB	SPARE							
WORD NO. 12	Y COORDINATE OF SLEW DOT									LSB	SPARE							
	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

NOTES:

* 1. CHARACTER CODES

* 2. EACH 7-BIT CHARACTER IS FORMATED AS FOLLOWS:

P	MSB					LSB

P IS PARITY BIT FOR EVEN PARITY

3. WORDS 11 AND 12 ARE OPTIONAL AT OPERATOR'S DISCRETION

4. ANY NUMBER OF ALPHANUMERICS (A/N'S) FROM 0 TO 15 MAY BE SELECTED BY THE OPERATOR

Table IV. Message Format (Message Generator Buffer to Display)

	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WORD NO. 1	CONSOLE BITS										SPARE				1	1		0
WORD NO. 2	±	X COORDINATE										LSB	SPARE					
WORD NO. 3	±	Y COORDINATE										LSB	SPARE					
WORD NO. 4	0	0	0	0	0	0	0	0	0	0	0	0	SPARE					0
WORD NO. 5	0	1	1	1	0	1	0	0/1	0/1	1	SPARE				0	0	0	0
WORD NO. 6	A/N NO. 3						A/N NO. 2						A/N NO. 1					
WORD NO. 7	A/N NO. 6						A/N NO. 5						A/N NO. 4					
WORD NO. 8	A/N NO. 9						A/N NO. 8						A/N NO. 7					
WORD NO. 9	A/N NO. 12						A/N NO. 11						A/N NO. 10					
WORD NO. 10	A/N NO. 15						A/N NO. 14						A/N NO. 13					
WORD NO. 11	SPARE						SPARE						0	0	0	0	1	1
	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

NOTES:

1. THIS FORMAT IS A VARIATION OF THE COMPUTER TO DISPLAY FORMAT.
2. THE ABOVE FIGURE IS FOR A MAXIMUM MESSAGE. MESSAGES WITH LESS THAN 15 A/N'S SHALL HAVE THE END OF FORMAT CHARACTER (SHOWN IN WORD NO. 1) FOLLOWING THE LAST A/N CHARACTER OF THE MESSAGE.
3. THE A/N CHARACTERS ARE CODED AS SPECIFIED BY FAA.
4. 0/1 INDICATES A DON'T CARE CONDITION FOR THIS BIT.

CONCLUSION

All work on contract No. FA-WA-4178 is proceeding on schedule and no difficulties are anticipated.

GPO 864-977